QSFP112
Multi-Source Agreement

Specification for

QUAD SMALL FORM FACTOR PLUGGABLE MODULE 112

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Abstract:

This specification defines the electrical connectors, electrical signals and power supplies, mechanical and thermal requirements of the QSFP112 module, connector and cage systems.

This document provides a common specification for system manufacturers, system integrators, and suppliers of modules.

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Revision	Date	Release	Remarks
1.0	June 10, 2021	1st public release	
2.0	January 10，2022	2nd public release	-Added chapter 5.9 for QSFP112 Qpath112 connector and cage definition. -Added Figure 18 and Figure 19 for QSFP112 Qpath112 2X1 connector and cage PCB layout. - Updated Figure 17 and Figure 24 for QSFP112 2X1 SMT connector and cage PCB layout.
2.1	August 24，2022	3rd public release	-Delete section 5.8.1 and update section 5.8, add Figure 25, 27, 29 and 30. -Update Figure 2, 24 and Figure 28. -Update table 10. -Update section 4.1.1.3
2.1.1	October 11, 2022	4th public release	-Update Figure 14.

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1 Scope

The scope of this specification covers the following items:

- The QSFP112 (4-channel, up to 112 Gbps per channel) transceiver module including mechanical form-factor, electrical interface, power specification, ect
- Host cage together with the host electrical connector mating with plug
- Electrical interface, including pin-out, data, control, power and ground signals
- Mechanical interface, including package outline, front panel and PCB layout requirements
- Thermal requirements and limitations, including heat-sink and airflow design
- Electrostatic discharge (ESD) requirements, and EMI requirements
- Software Management Interface.

2 Reference

- ANSI/ESDA/JEDEC JS-001-2014: Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) - Component Level
- CMIS (Common Management Interface Specifications) 5.1, see http://www.qsfp-dd.com
- EN61000-4-2:2008: Electromagnetic compatibility (EMC)- Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test
- IEEE P802.3ck™/D1.5 Draft Standard for Ethernet Amendment: Physical Layer Specifications and Management Parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Based on 100 Gb/s Signaling
- IEEE P802.3db™/D1.0 Draft Standard for Ethernet Amendment: Physical Layer Specifications and Management Parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s Operation over Optical Fiber using 100 Gb/s Signaling
- OIF CEI-112G-VSR-PAM4 draft, Rev. 2017.346.15
- QSFP-DD Hardware Specification Rev.6.0
- QSFP-DD800 Specification Rev.1.0
- SFF-8024 SFF Module Management Reference Code Tables, Rev. 4.7
- SFF-8661 Specification for QSFP+ 4X Module, Rev2.5
- SFF-8636 Specification for Management Interface for 4-lane Modules and Cables, Rev. 2.10a
- SFF-8662 Specification for QSFP+ 4X 28 Gb/s Connector (Style A), Rev 2.9
- SFF-8663 Specification for QSFP+ 28 Gb/s Cage (Style A), Rev 1.7
- SFF-8665 QSFP+ 4X 28 Gb/s Pluggable Transceiver Solution (QSFP28), Rev 1.9
- SFF-8679 QSFP28 4X Base Electrical Specification, Rev 1.8
- Telcordia GR-63-CORE, Issue 5, December 2017

Each Participant acknowledges the Specifications will provide a common solution for combined four-channel fiber optic ports that support SONET/SDH and/or Ethernet and/or Fiber Channel specifications. This MSA encompasses module design(s) capable of supporting multimode and single mode applications for operation covering the transmission rates and distances noted below. Other standards covering higher data rates and/or longer distance options are not part of this agreement but may be supported. A QSFP112 module may support applications in Table 1 and Table 2 that are supplied for reference only.

Table 1 Multimode fiber applications

PMD type	Required operating range
VR	0.5m to 30m for OM3
	0.5m to 50m for OM4
	0.5m to 50m for OM5
SR	0.5m to 60m for OM3
	0.5m to 100m for OM4
	0.5m to 100m for OM5

Table 2 Single mode fiber applications

PMD type	Required operating range
DR	2m to 500m
FR	2m to 2km
LR	2m to 10km
ER	2m to 40km
ZR	2m to 80km

3 QSFP112 Application Reference Examples

This specification defines a common four-lanes pluggable module that uses the following application reference Model. An Application Reference Model, shown in Figure 1, shows the high-speed data interface between an ASIC (SerDes) and the QSFP112 module.

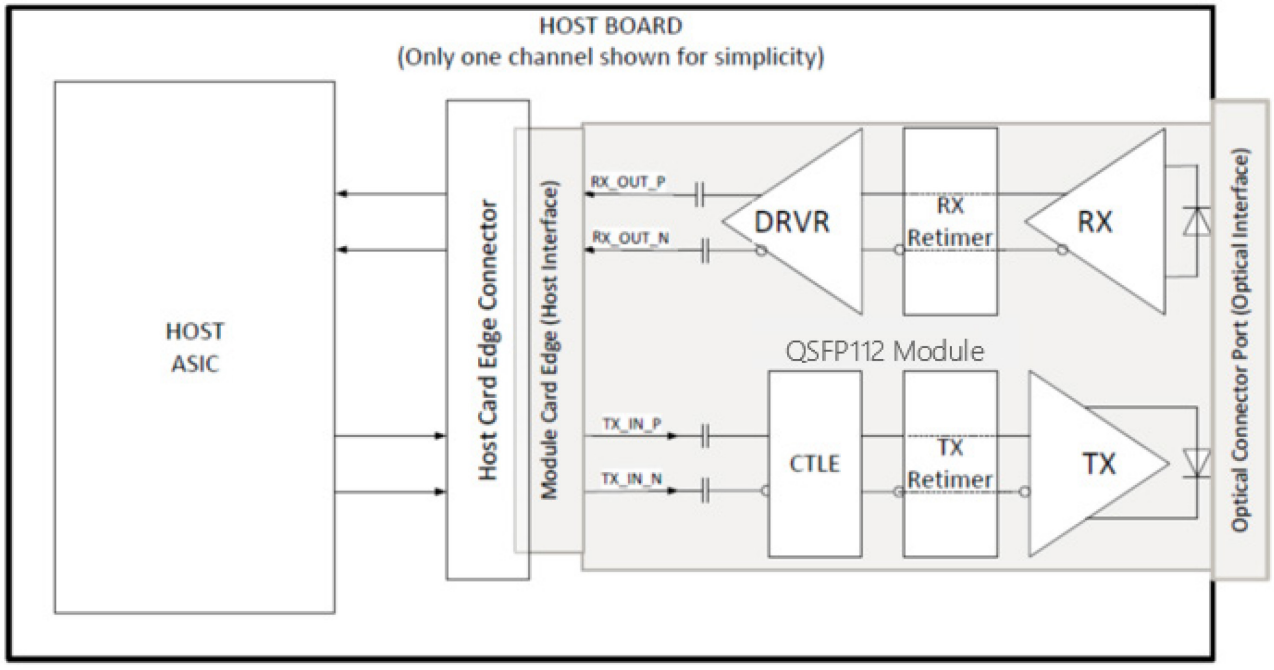


Figure 1 Application reference model

4 Electrical Interface

4.1 Electrical Connector

The QSFP112 connector is a 38-contact connector.

QSFP112 module contacts mate with the host in the order of ground, power, followed by signal as illustrated by Figure 2 and Figure 3 and the contact sequence order listed in Table 3.

Figure 2 QSFP112 Module contact assignment

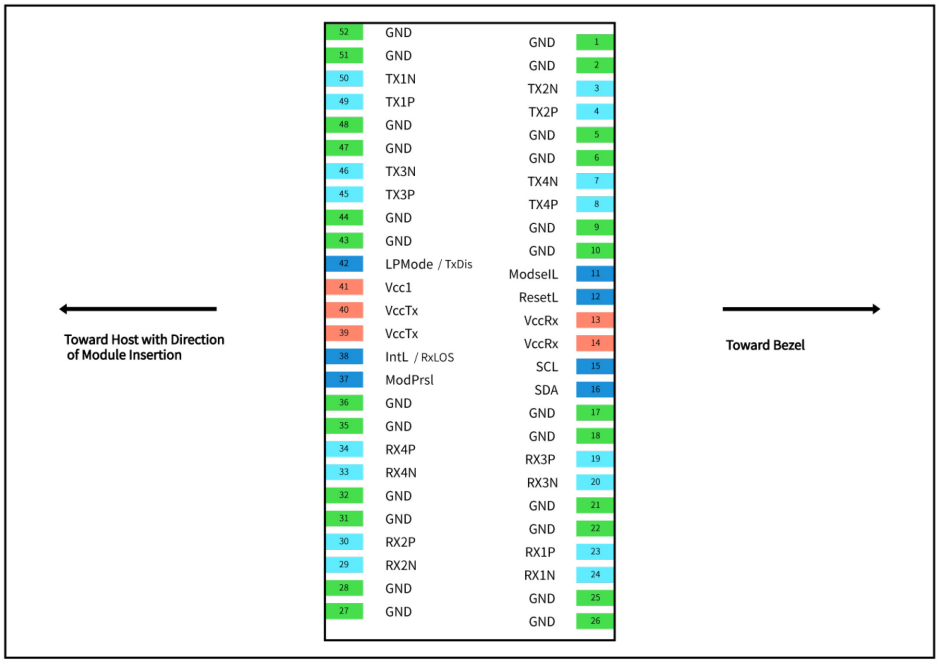


Figure 3 QSFP112 Host PCB pad assignment

Table 3 QSFP112 Module contact and Host PCB pad electrical definition

Host PCB pad	Module contact	Logic	Symbol	Description	Plug Sequence	Notes
1	1		GND	Ground	1	1
2			GND	Ground	1	1
3	2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
4	3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
5	4		GND	Ground	1	1
6			GND	Ground	1	1
7	5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
8	6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
9	7		GND	Ground	1	1
10			GND	Ground	1	1
11	8	LVTTL-I	ModSelL	Select	3	
12	9	LVTTL-I	ResetL	Reset	3	
13	10		Vcc Rx	+3.3 V Power supply receiver	2	2
14			Vcc Rx	+3.3 V Power supply receiver	2	2
15	11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
16	12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
17	13		GND	Ground	1	1
18			GND	Ground	1	1
19	14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
20	15	CML-O	Rx3n	Receiver Inverted Data Output	3	
21	16		GND	Ground	1	1
22			GND	Ground	1	1
23	17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
24	18	CML-O	Rx1n	Receiver Inverted Data Output	3	
25	19		GND	Ground	1	1
26			GND	Ground	1	1
27	20		GND	Ground	1	1
28			GND	Ground	1	1
29	21	CML-O	Rx2n	Receiver Inverted Data Output	3	
30	22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
31	23		GND	Ground	1	1
32			GND	Ground	1	1
33	24	CML-O	Rx4n	Receiver Inverted Data Output	3	
34	25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
35	26		GND	Ground	1	1
36			GND	Ground	1	1
37	27	LVTTL-O	ModPrsL	Present	3	
38	28	LVTTL-O	IntL/RxLOS	Interrupt/optional RxLOS	3	
39	29		Vcc Tx	+3.3 V Power supply transmitter	2	2
40			Vcc Tx	+3.3 V Power supply transmitter	2	2
41	30		Vcc1	+3.3 V Power Supply	2	2
42	31	LVTTL-I	LPMode/Tx Dis	Low Power Mode/optional TX Disable	3	
43	32		GND	Ground	1	1
44			GND	Ground	1	1
45	33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
46	34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
47	35		GND	Ground	1	1
48			GND	Ground	1	1
49	36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	

50	37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
51	38		GND	Ground	1	1
52			GND	Ground	1	1
Note 1: GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.						
Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements, defined for the host side of the Host Edge Card Connector, are listed in Table 4. Recommended host board power supply filtering is shown in Figure 4. Vcc Rx, Vcc1and Vcc Tx may be internally connected within the QSFP112 module in any combination. The connector pins are each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W).						

Figure 4, Figure 5 and Figure 6 show example of QSFP host PCB schematic with connections to CDR and control ICs.

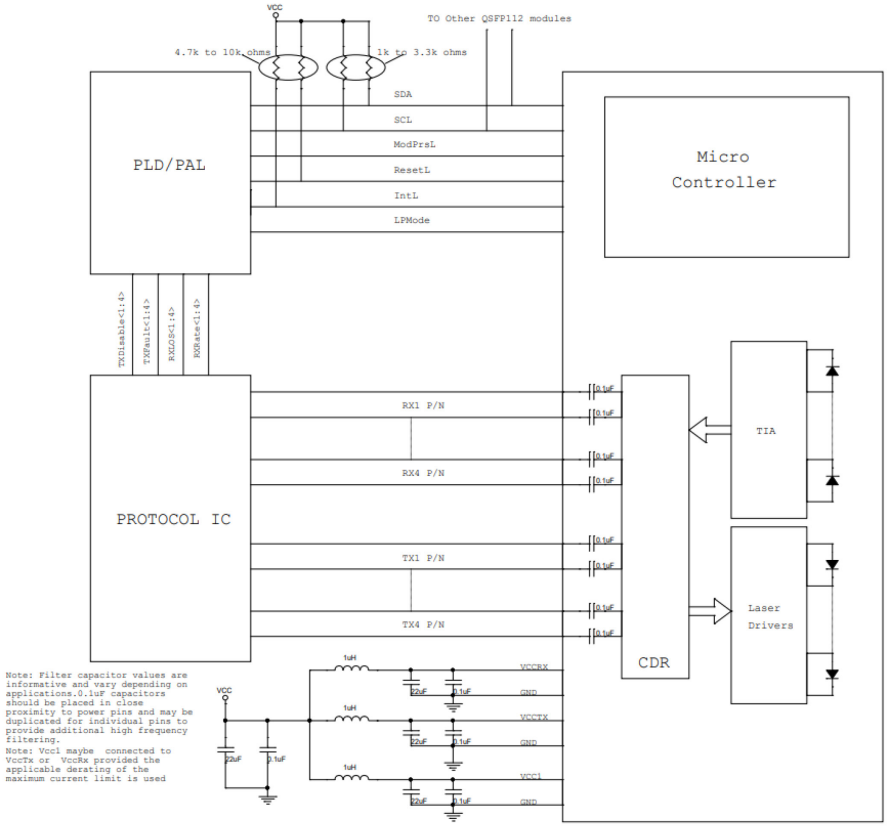


Figure 4 Example QSFP112 host board schematic for optical modules

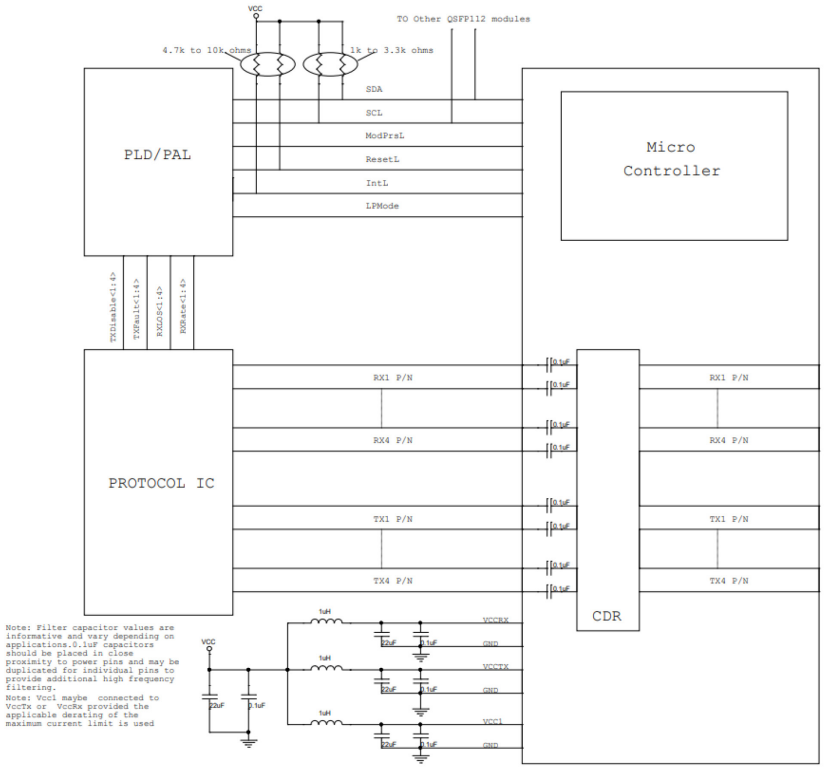


Figure 5 Example QSFP112 host board schematic for active copper cables

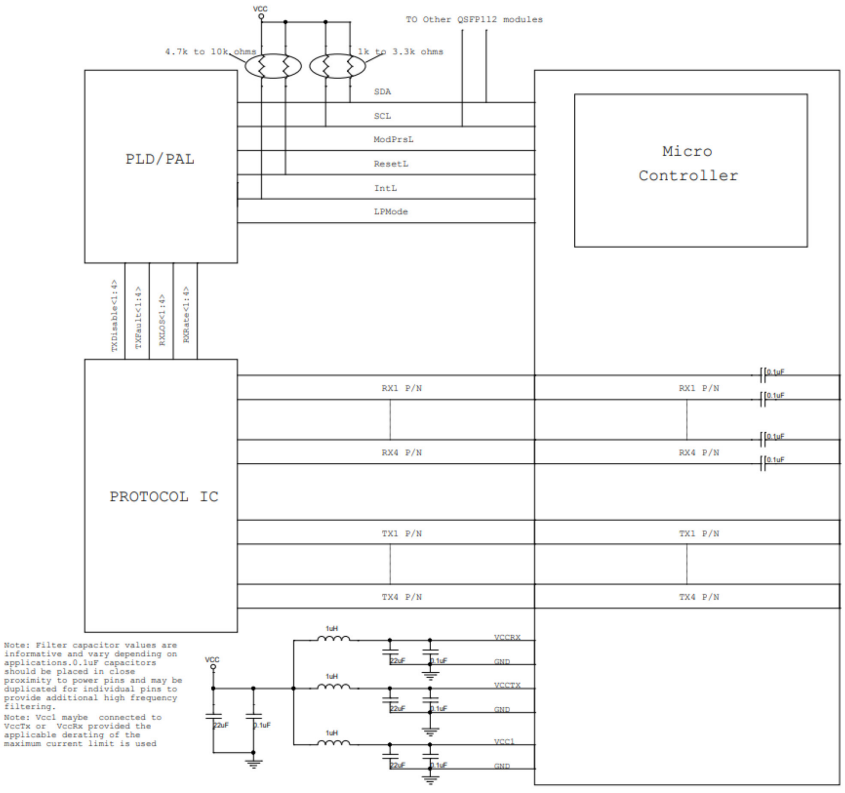


Figure 6 Example QSFP112 host board schematic for passive copper cables

4.1.1 Low Speed Electrical Hardware Pins

In addition to the two wire interface (TWI) serial interface the module has the following low speed pins for control and status:

a) ModSelL
b) LPMode/TxDis
c) ResetL
d) ModPrsL
e) IntL/RxLOSL

4.1.1.1 ModSelL

The ModSelL is an input pin. When held low by the host, the module responds to TWI serial communication commands. The ModSelL allows the use of multiple QSFP112 modules on a single TWI bus. When the ModSelL is "High", the module shall not respond to or acknowledge any TWI communication from the host. ModSelL signal input node must be biased to the "High" state in the module.

In order to avoid conflicts, the host system shall not attempt TWI communications within the ModSelL de-assert time after any QSFP112 modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

4.1.1.2 ResetL

The ResetL pin must be pulled to Vcc in the QSFP112 module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

4.1.1.3 LPMode/TxDis

LPMode/TxDis is a dual-mode input signal from the host operating with active high logic. It shall be pulled towards Vcc in the module. At power-up or after ResetL is deasserted LPMode/TxDis behaves as LPMode. If supported, LPMode/TxDis can be configured as TxDis using the TWI except during the execution of a reset. Timing requirements for LPMode/TxDis mode changes are found in, see Table 15. LPMode is used in the control of the module power mode, see CMIS Chapter 6.3.1.3.

When LPMode/TxDis is configured as LPMode, the module behaves as though TxDis=0. By using the LPMode signal and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits the host controls how much power a module can consume. When LPMode/TxDis is configured as TxDis, the module behaves as though LPMode=0. In this mode LPMode/TxDis when set to 1 or 0 disables or enables all optical transmitters within the times specified in Table 15.

Changing LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is high disables all optical transmitters. If the module was in low power mode, then the module transitions out of low power mode at the same time. If the module is already in high power state (Power Override control bits) with transmitters already enabled, the module shall disable all optical transmitters. Changing the LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is low, simply changes the behavior of the mode of LPMode/TxDis. The behavior of the module depends on the Power Override control bits.

Note that the "soft" functions of TxDis, LPMode, IntL and RxLOSL allow the host to poll or set these values over the TWI as an alternative to monitoring/setting signal values. Asserting either the "hardware" or "soft bit" (or both) for TxDis or LPMode results in that function being asserted.

4.1.1.4 ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

4.1.1.5 IntL/RxLOSL

IntL/RxLOSL is a dual-mode active-low, open-collector output signal from the module. It shall be pulled up towards Vcc on the host board (see Table 4). At power-up or after ResetL is released to high, IntL/RxLOSL is configured as IntL. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the TWI serial interface. The IntL signal is deasserted "High" after all set interrupt flags are read. If dual mode operation supported, IntL/RxLOSL can be optionally programmed as RxLOSL using the TWI except during the execution of a reset. If the module has no interrupt flags asserted (IntL/RxLOSL is high), there should be no change in IntL/RxLOSL states after the mode change. If IntL/RxLOSL is configured as RxLOSL, a low indicates that there is a loss of received optical power on at least one lane. "high" indicates that there is no loss of received optical power. Timing requirements for IntL/RxLOSL including fast RxLOS mode are found in Table 15. The actual condition of loss of optical receive power is specified by other governing documents, as the alarm threshold level is application specific. The module shall pull RxLOSL to low if any lane in a multiple lane module or cable has a LOS condition and shall release RxLOSL to high only if no lane has a LOS condition.
Editor' s Note: registers to support optional RxLOSL will be added in future revisions of CMIS.

4.1.2 Low Speed Electrical Specification

Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc_host or Vcc1. Hosts shall use a pull-up resistor connected to Vcc_host on each of the TWI SCL (clock), SDA (data), and all low speed status outputs. The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.
The QSFP112 low speed electrical specifications are given in Table 4. This specification ensures compatibility between host bus masters and the TWI.

Table 4 Low speed control and sense signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max) = 3.0 mA for fast mode, 20 mA for Fast-mode plus
	VOH	Vcc - 0.5	Vcc + 0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc + 0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	3.0 k Ohms Pull up resistor, max
			200	pF	1.6 k Ohms Pull up resistor, max
LPMode/TxDis, Reset and ModeSelL	VIL	-0.3	0.8	V	| Iin | </= 125 uA for 0V < Vin < Vcc
	VIH	2	VCC + 0.3	V	
IntL/RxLOS	VOL	0	0.4	V	IoL= 2.0 mA
	VOH	VCC - 0.5	VCC + 0.3	V	10 k ohms pull-up to Host Vcc
ModPrsL	VOL	0	0.4	V	IoL= 2.0 mA
	VOH				ModPrsL can be implemented as a short-circuit to GND on the module

4.1.3 High Speed Electrical Specification

4.1.3.1 Rx(n)(p/n)

Rx(n)(p/n) are QSFP112 module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the QSFP112 module and not required on the Host board. When properly terminated, the differential voltage swing shall be less than or equal to 900 mVpp or the relevant standard, whichever is less.

Output squelch for loss of optical input signal, hereafter Rx Squelch, is required and shall function as follows. In the event of the Rx input signal on any optical port becoming equal to or less than the level required to assert LOS, then the receiver output(s) associated with that Rx port shall be squelched. A single Rx optical port can be associated with more than one Rx output. In the squelched state output impedance levels are maintained while the differential voltage amplitude shall be less than 50 mVpp.

In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the TWI serial interface. Rx Squelch Disable is an optional function.

4.1.3.2 Tx(n)(p/n)

Tx(n)(p/n) are QSFP112 module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the QSFP112 optical module. The AC coupling is implemented inside the QSFP112 optical module and not required on the Host board.

Output squelch for loss of electrical signal, hereafter Tx Squelch, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal amplitude on any electrical input channel becoming less than 70 mVpp, then the transmitter optical output associated with that electrical input channel shall be squelched and the associated TxLOS flag set. If multiple electrical input channels are associated with the same optical output channel, the loss of any of the incoming electrical input channels causes the optical output channel to be squelched.

For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, squelching by disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter by setting the OMA to a low level is recommended.

In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the TWI serial interface. Tx Squelch and Tx Squelch Disable are optional functions.

4.2 Power Requirements

The power supply has three designated pins, Vcc Tx, Vcc1, and Vcc Rx, in the connector. Vcc1 is used to supplement Vcc Tx or Vcc Rx at the discretion of the module vendor. Power is applied concurrently to these pins.

Since different classes of modules exist with pre-defined maximum power consumption limits, it is necessary to avoid exceeding the system power supply limits and cooling capacity when a module is inserted into a system designed to only accommodate lower power modules. It is recommended that the host, through the management interface, identify the power consumption class of the module before allowing the module to go into high power mode.

A host board together with the QSFP112 module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion.

All specifications shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.

4.2.1 Host Board Power Supply Filtering

The host board should use the power supply filtering shown in Figure 7.

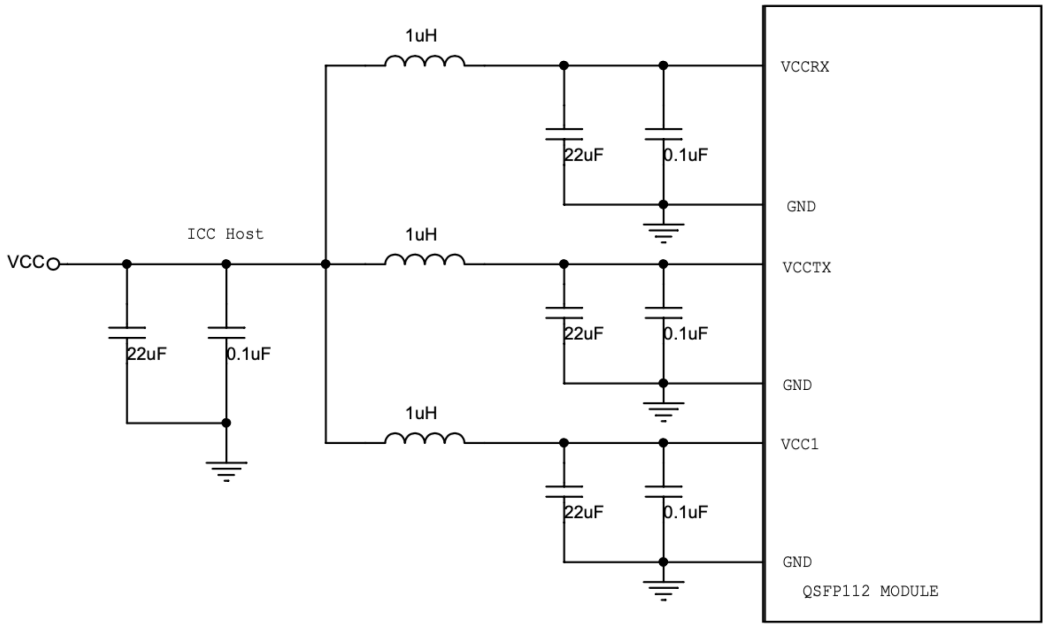


Figure 7 Recommended host board power supply filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used to maintain the required voltage at the Host Edge Card Connector.

The specification for the power supply is shown in Table 5.

Table 5 Power supply specification

Parameter	Min	Nominal	Max	Unit	Condition
Vcc		3.3		V	Measured at Vcc Tx, Vcc Rx and Vcc1.
Vcc set point accuracy	-5		5	%	Measured at Vcc Tx, Vcc Rx and Vcc1.
Power Supply Noise including ripple			50	mV	1 kHz to frequency of operation measured at Vcc_host.
Module Maximum Current Inrush with LPMode Pin asserted			0.55	A	
Module Maximum Current Inrush with LPMode Pin deasserted			1.3	A	
Module Current Ramp Rate			100	mA/uS	

4.2.2 Power Classes and Maximum Power Consumption

Power levels associated with classifications of module are shown in Table 6.

Since a wide range of module power classes exist, to avoid exceeding the system power supply limits and cooling capacity when a module is inserted into a system designed to accommodate only low power consumption modules, it is recommended that host systems designed to accommodate only low power consumption modules also implement the state machine defined in the CMIS or SFF-8636 and identify the power class of the module before allowing the module to go into High Power Mode, where power class 8 requires reading CMIS, Page00, Byte 201 to determine actual power consumption. This is to avoid exceeding the host system power supply limits and cooling capacity when a module exceeding the power class supported by the system is inserted.

Table 6 Power budget classification

Power Class	Max Power (W)	CMIS Register
1	1.5	Direct readout of Page 00h Byte 200[000xxxxx]
2	2.0	Direct readout of Page 00h Byte 200[001xxxxx]
3	2.5	Direct readout of Page 00h Byte 200[010xxxxx]
4	3.5	Direct readout of Page 00h Byte 200[011xxxxx]
5	4.0	Direct readout of Page 00h Byte 200[100xxxxx]
6	4.5	Direct readout of Page 00h Byte 200[101xxxxx]
7	5.0	Direct readout of Page 00h Byte 200[110xxxxx]
8 [1]	>5.0	Direct readout of Page 00h Byte 200[111xxxxx]
Note: 1. When a module reports power class 8, the host must read CMIS Page 00h Byte 201 to determine module power dissipation.		

In general, the higher power classification level is associated with higher data rates and longer reach. The system designer is responsible for ensuring that the maximum temperature does not exceed the case temperature requirements.

During hot-plug, power cycle or reset, all QSFP112 modules shall power up in Low Power Mode if LPMode is asserted to avoid exceeding the host system power capacity. If LPMode is not asserted, the module will proceed to High Power Mode without host intervention. Figure 8 shows waveforms for maximum instantaneous, sustained and steady state currents for Low Power and High Power modes.

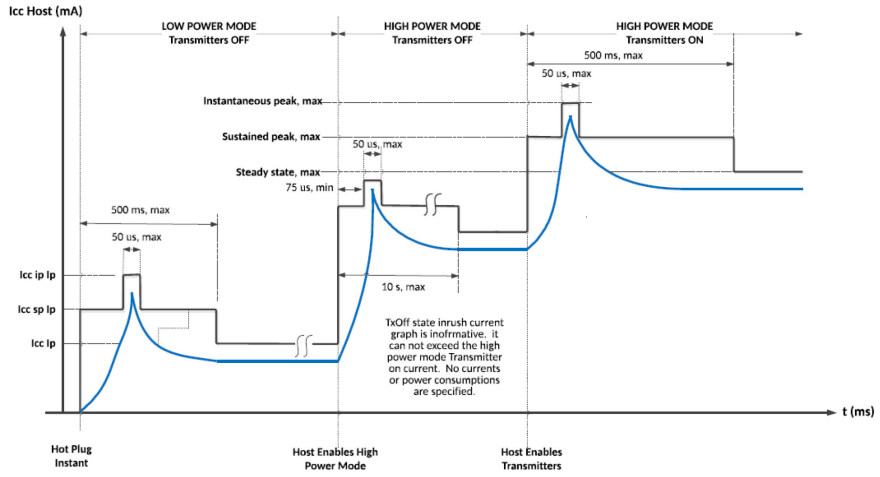


Figure 8 Instantaneous and sustained peak currents for icc host

Specification values for maximum instantaneous, sustained and steady state currents at each power class are given in Table 7. The module shall not be affected by the instantaneous variations of the power supply caused by its own current drawing profile during all power transient events.

Table 7 QSFP112 Module power supply specification

Parameter	Symbol	Min	Nom	Max	Unit
Power supply voltages VccTx, VccRx, including ripple, droop and noise below 100 kHz[1]		3.135	3.3	3.465	V
Module inrush - instantaneous peak duration[2]	T_ip			50	µs
Module inrush - initialization time[2]	T_init			500	ms
Power Class 1 module and Low Power Mode for other modules					
Power Consumption	P_lp			1.5	W
Instantaneous peak current at hot plug	Icc_ip_lp	-	-	600	mA
Sustained peak current at hot plug	Icc_sp_lp	-	-	495	mA
Steady state current	Icc_lp		See Note 3		mA
High Power Mode Power Class 2 module					
Power Consumption	P_2			2.0	W
Instantaneous peak current	Icc_ip_2	-	-	800	mA
Sustained peak current	Icc_sp_2	-	-	660	mA
Steady state current	Icc_2		See Note 3		mA
High Power Mode Power Class 3 module					
Power Consumption	P_3			2.5	W
Instantaneous peak current	Icc_ip_3	-	-	1000	mA
Sustained peak current	Icc_sp_3	-	-	825	mA
Steady state current	Icc_3		See Note 3		mA
High Power Mode Power Class 4 module					
Power Consumption	P_4			3.5	W
Instantaneous peak current	Icc_ip_4	-	-	1400	mA
Sustained peak current	Icc_sp_4	-	-	1155	mA
Steady state current	Icc_4		See Note 3		mA
High Power Mode Power Class 5 module					
Power Consumption	P_5			4.0	W
Instantaneous peak current	Icc_ip_5	-	-	1600	mA
Sustained peak current	Icc_sp_5	-	-	1320	mA
Steady state current	Icc_5		See Note 3		mA
High Power Mode Power Class 6 module					
Power Consumption	P_6			4.5	W
Instantaneous peak current	Icc_ip_6	-	-	1800	mA
Sustained peak current	Icc_sp_6	-	-	1485	mA
Steady state current	Icc_6		See Note 3		mA
High Power Mode Power Class 7 module					
Power Consumption	P_7			5	W
Instantaneous peak current	Icc_ip_7	-	-	2000	mA
Sustained peak current	Icc_sp_7	-	-	1650	mA
Steady state current	Icc_7		See Note 3		mA
High Power Mode Power Class 8 module					
Power Consumption	P_8			> 5	W
Instantaneous peak current	Icc_ip_8	-	-	P_8/2.5	A
Sustained peak current	Icc_sp_8	-	-	P_8/3.03	A
Steady state current	Icc_8		6.0		A

Notes: 1. Measured at VccTx, VccRx and Vcc1.

2: T_ip and T_init are test conditions for measuring inrush current and not characteristics of the module.

3: The module must stay within its declared power class.

4: P_8 is the module power dissipation reported by CMIS Byte 201.

4.3 ESD

The module and all pins shall withstand 500V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.
The module shall meet ESD requirements given in EN61000-4-2, criterion B test specification such that when installed in a properly grounded cage and chassis the units are subjected to 15KV air discharges during operation and 8KV direct contact discharges to the case.

5 Mechanical and Board Definition

5.1 Introduction

The overall module defined in this clause is illustrated in Figure 9. The module and connector dimensions described in this clause are constant for all applications. The bezel, cage assembly, heat sink can be designed and/or adjusted for the individual application.

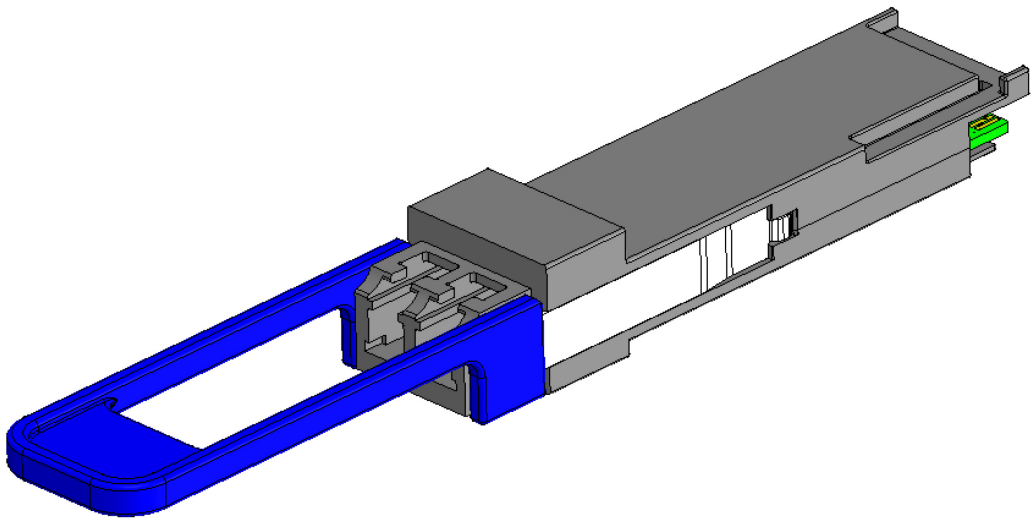


Figure 9 QSFP112 Module rendering

5.2 QSFP112 Datums and Component Alignment

A listing of the datums for the various components is contained in Table 8. The alignments of some of the datums are noted. The relationship of the Module, Cage, and Connector relative to the Host Board and Bezel are illustrated in Figure 10 and Figure 11 by the location of the key datums of each of the components. In order to reduce the complexity of the drawings, all dimensions are considered centered unless otherwise specified.

Table 8 Definition of datums

Datum	Description
A	Top surface of Host Board
B	Inside surface of bezel
C	Distance between connector terminal through holes on host board
D	Hard stop on module
E	Width of module
F	Height of module housing
G	Width of PCB
H	Leading edge of signal contact pads on PCB
J	Top surface of PCB
K	Host Board through hole #1 to accept contact guide post
L	Host Board through hole #2 to accept contact guide post
P	Centerline of cage width
R	Centerline of cage height
S	Seating plane of cage on host board
T	Hard stop on cage
W	Seating surface of the heat sink on the cage
X	Host board through hole #1 to accept cage pin
Z	Width of heat sink surface that fits into clip
AA	Connector slot width
BB	Seating plane of connector on host board
DD	Top surface of module housing

Notes:

1. Datums D, K, L, N and T are aligned when assembled
2. Centerlines of datums AA,C,E,G,M,P and Z are aligned on the same vertical axis

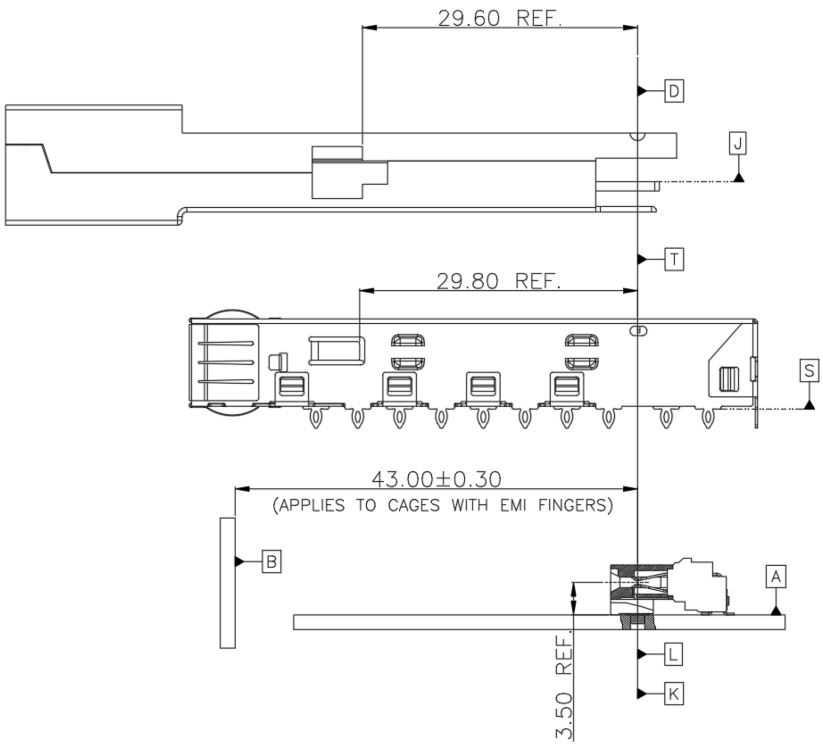


Figure 10 QSFP112 1X1 SMT Connector/Cage/Module Datum

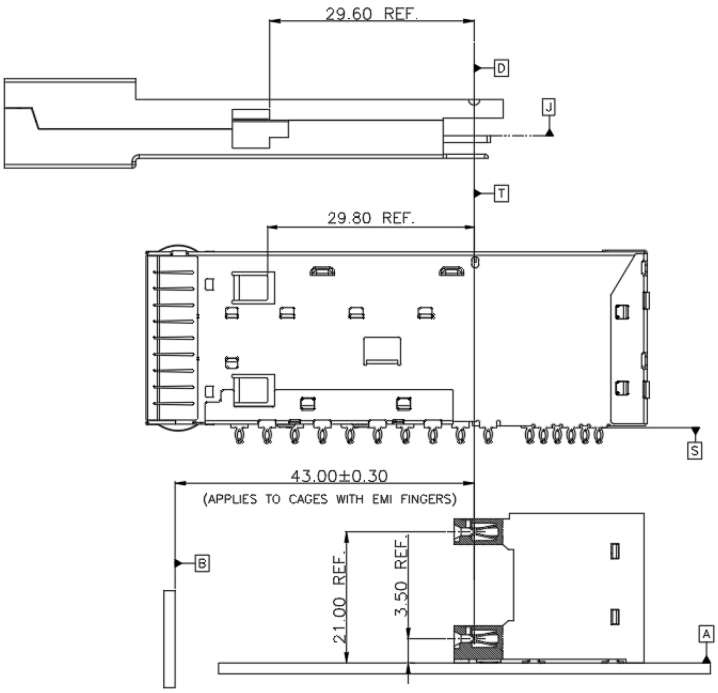


Figure 11 QSFP112 2X1 SMT Connector/Cage/Module Datum

5.3 QSFP112 Module Mechanical Package Dimensions

5.3.1 Module Form Factors

A common mechanical outline is used for all QSFP112 modules. The shell provides a means to self-lock with the cage upon insertion. The package dimensions for the QSFP112 module are defined in Figure 12 and Figure 13. The dimensions that control the size of the module that extends outside of the cage are listed as maximum dimensions per below Note 4 and Note 8 in Figure 12.

NOTES APPLY TO MODULE DRAWING

1. DIMENSIONS AND TOLERANCING CONFORM TO ASME Y14.5-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. UNLESS OTHERWISE SPECIFIED, SHARP CORNERS, EDGES, AND BURRS ARE NOT ALLOWED. ROUND OFF ALL EDGES AND CORNERS TO A MINIMUM RADIUS OF 0.2MM.
4. DIMENSIONS DEFINES ENLARGED SECTION OF TRANSCEIVER THAT EXTENDS OUTSIDE OF CAGE TO ACCOMMODATE MATING PLUG AND ACTUATOR MECHANISM.
5. SURFACES ON ALL 4 SIDES OF THE 12.4 MIN DIMENSION TO BE CONDUCTIVE FOR CONNECTION TO CHASSIS GROUND.
6. DIMENSION APPLIES TO LATCH MECHANISM.
7. DIMENSION APPLIES TO THE LOCATION OF THE EDGE OF THE MODULE BOARD PAD, DATUM H. CONTACTS 21, 22, 36, AND 37 ARE VISIBLE.
8. DIMENSION TO INCLUDE BAIL TRAVEL.
9. DIMENSION APPLY TO OPENNINGS IN THE HOUSING.
10. FEATURE MAY BE LONGER THAN SHOWN.
11. FLATNESS AND SURFACE ROUGHNESS (Ra) APPLIES FOR INDICATED LENGTH AND MIN WIDTH OF 13MM. SURFACE TO BE THERMALLY CONDUCTIVE. SEE SECTION 5.3.2 TABLE 9 FOR FLATNESS AND ROUGHNESS REQUIREMENS.
12. HIGH WATTAGE MODULES MAY REQUIRE ADDITIONAL SPACE FOR COOLING.
13. NO LABEL SHALL BE APPLIED IN THIS AREA FOR TYPE 2/2A/2B. ETCHINGS ARE ALLOWED BUT MUST NOT AFFECT THERMAL PERFORMANCE.
14. THE LABEL(S) MUST NOT INTERFERE WITH THE MECHANICAL, THERMAL, OR EMI PERFORMANCE AND MUST NOT VIOLATE NOTE 5.

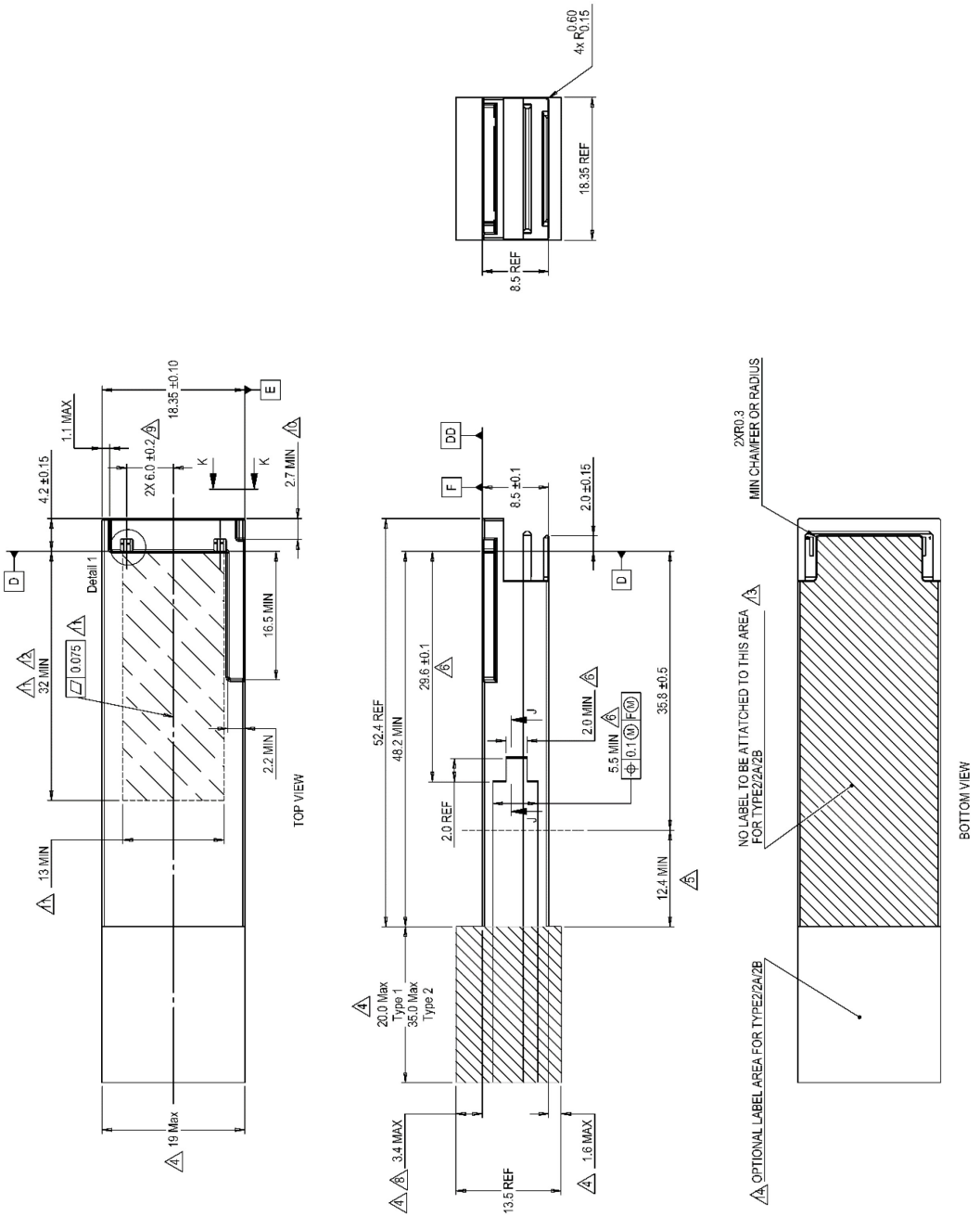


Figure 12 Drawing of QSFP112 module (Part 1 of 2)

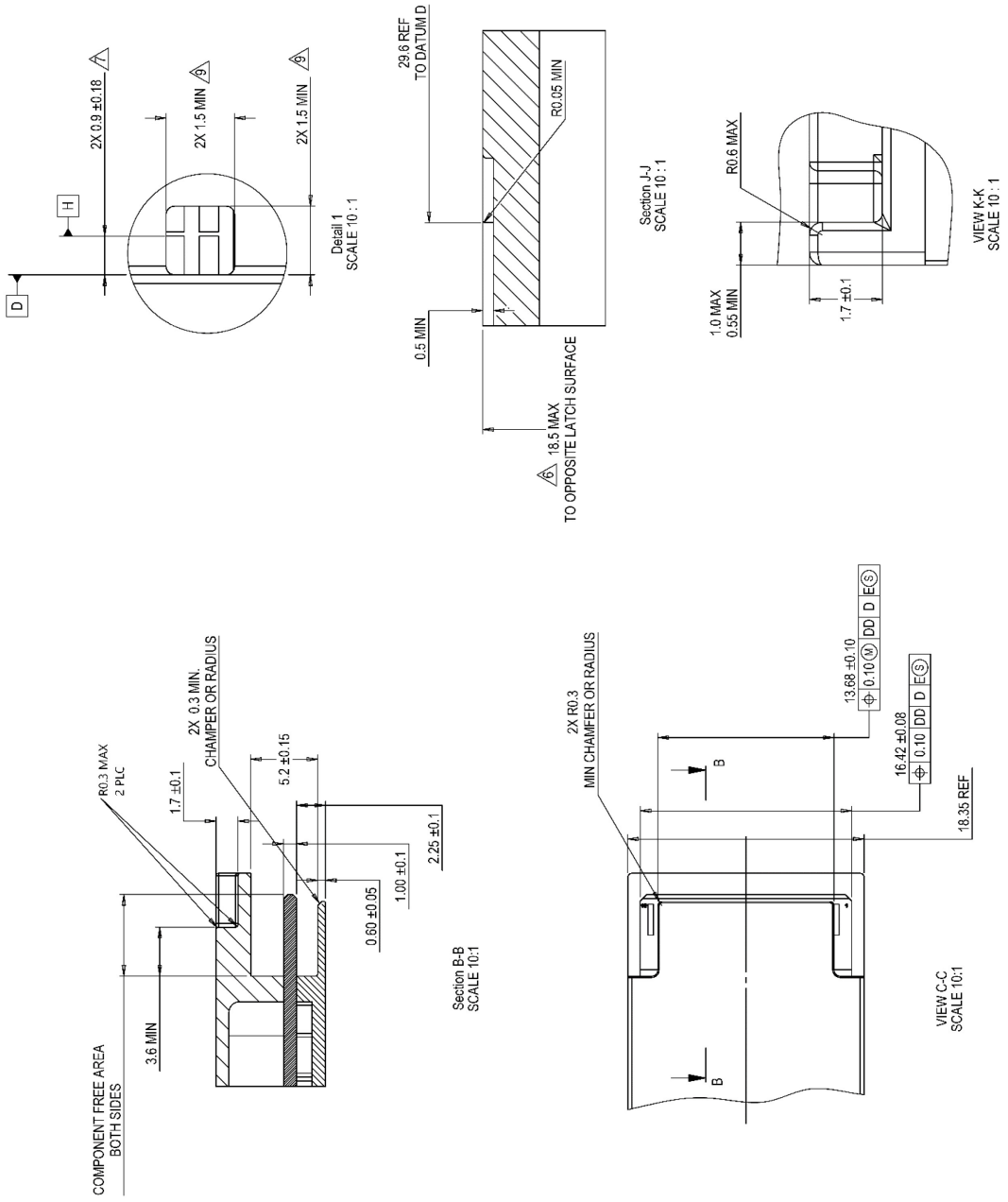


Figure 13 Drawing of QSFP112 module (Part 2 of 2)

5.3.2 Module Flatness and Roughness

QSFP112 module flatness and roughness are specified to improve module thermal characteristics when used with a riding heat sink. Relaxed specifications are used for lower power modules to reduce cost. The module flatness and roughness specifications apply to the specified heat sink contact area for QSFP112 by Figure 12 and Figure13. Specifications for QSFP112 Module flatness and surface roughness are shown in Table 9. Flatness and roughness specifications applies to both top and bottom surfaces of the modules. Power class 1Cu is dedicated to passive copper cables with a more relaxed flatness of 0.15 mm.

Table 9 QSFP112 Module flatness specifications

Power Class[1]	Module Flatness (mm)	Surface Roughness (Ra, μm)
1Cu[2]	0.15	1.6
1	0.075	1.6
2	0.075	1.6
3	0.075	1.6
4	0.075	1.6
5	0.075	1.6
6	0.075	1.6
7	0.075	1.6
8	0.050	0.8
1. QSFP112 power classes are defined in Table 6. 2. Power class 1Cu maximum power dissipation is the same as power class 1.		

5.3.3 Mating of QSFP112 Module PCB to QSFP112 Electrical Connector

The pad definition data is generic for high speed datacom applications such as Fiber Channel, Ethernet and SONET/ATM.

To support 112 Gb/s serial data rates the QSFP112 module paddle card pad dimensions have been modified. See Figure 14 for QSFP112 module updated paddle card pad dimensions, which uses 0.45 mm in width and 1.4mm in length. All other module dimensions, except for the pads, remain the same as the QSFP+/QSFP28 specifications.

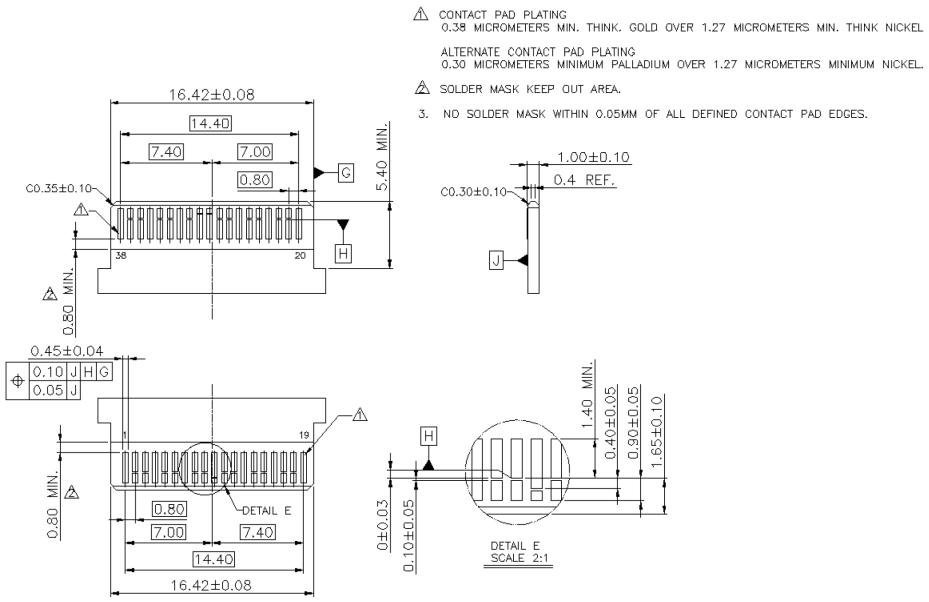


Figure 14 QSFP112 Improved paddle card dimensions

5.4 Host PCB Layout

A typical host board mechanical layout of single mount for attaching the QSFP112 Connector and Cage System is shown in Figure 15 , Figure 16, Figure 17, Figure 18 and Figure 19, the connector and the cage can also support belly to belly application of host board. Location of the pattern on the host board is application specific. See Clause 4.6 for details on the location of the pattern relative to the bezel.

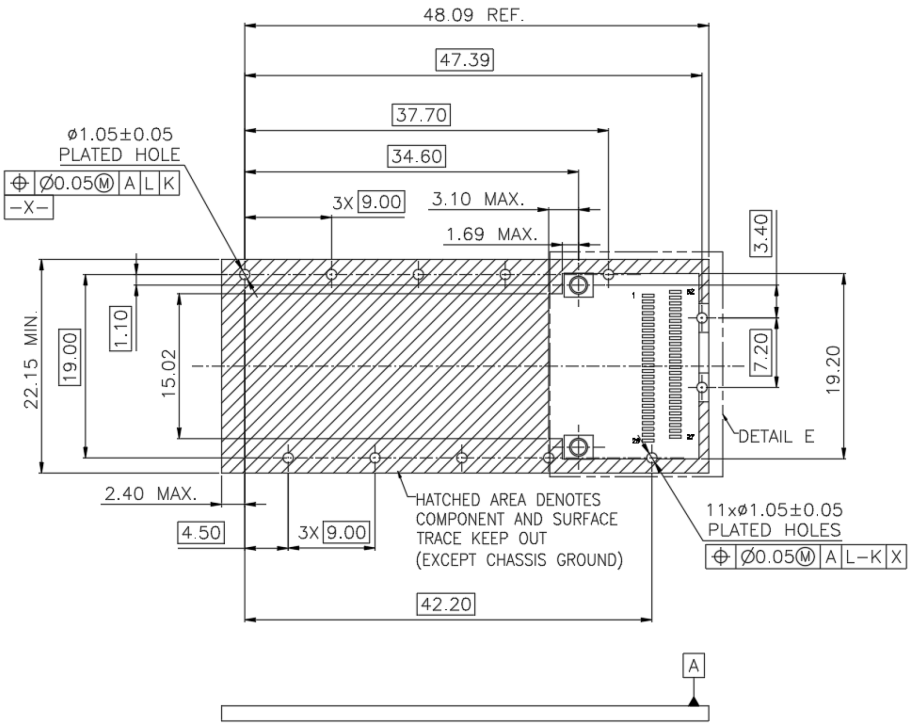


Figure 15 QSFP112 1x1 SMT Connector and cage PCB layout

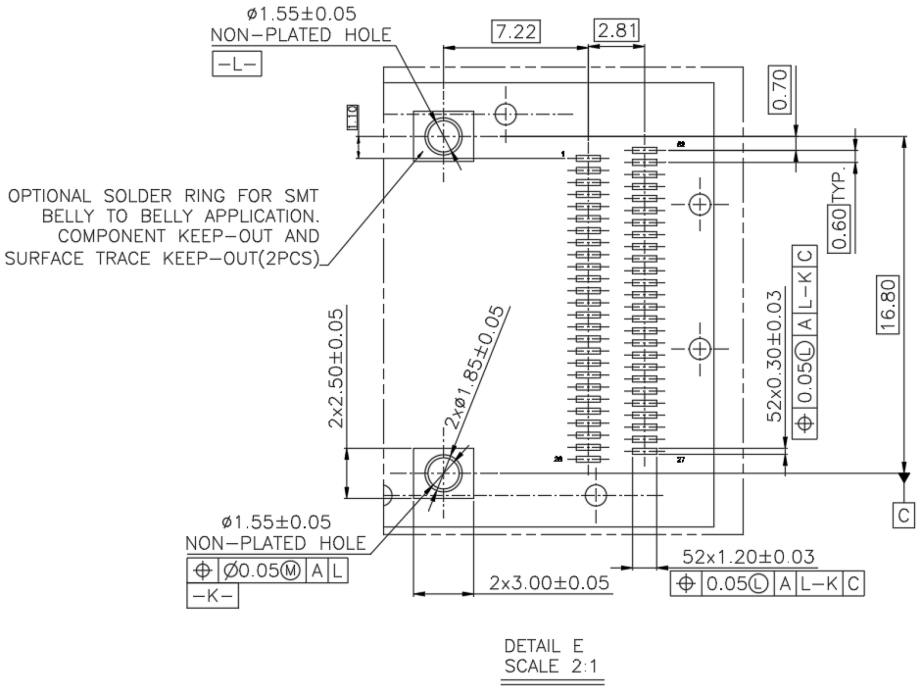


Figure 16 QSFP112 1x1 SMT Connector and cage PCB layout, Detail E

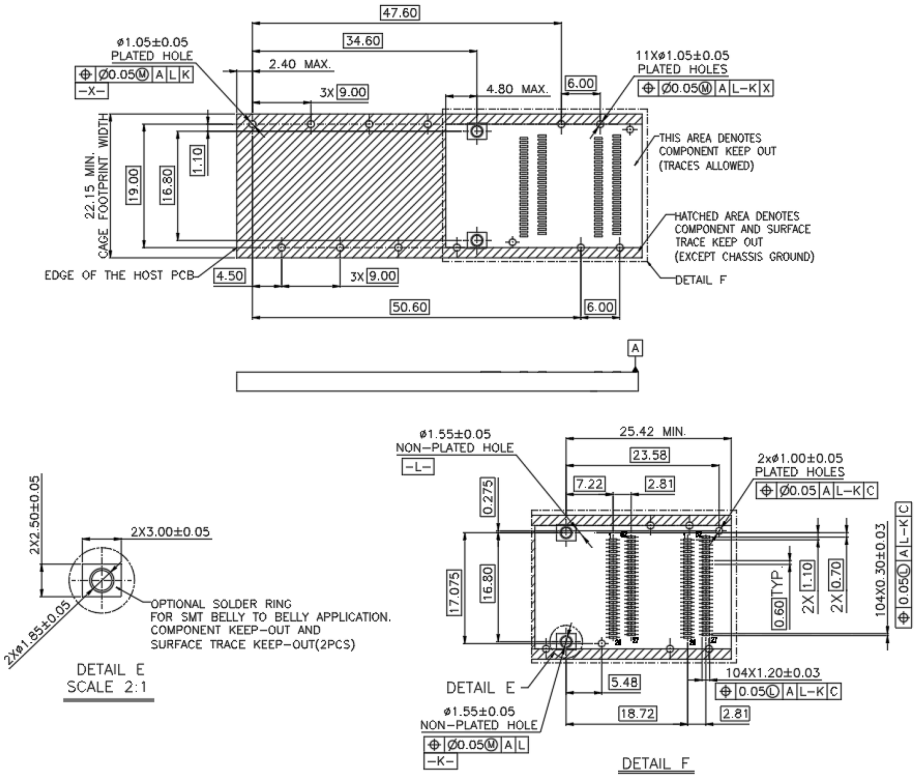
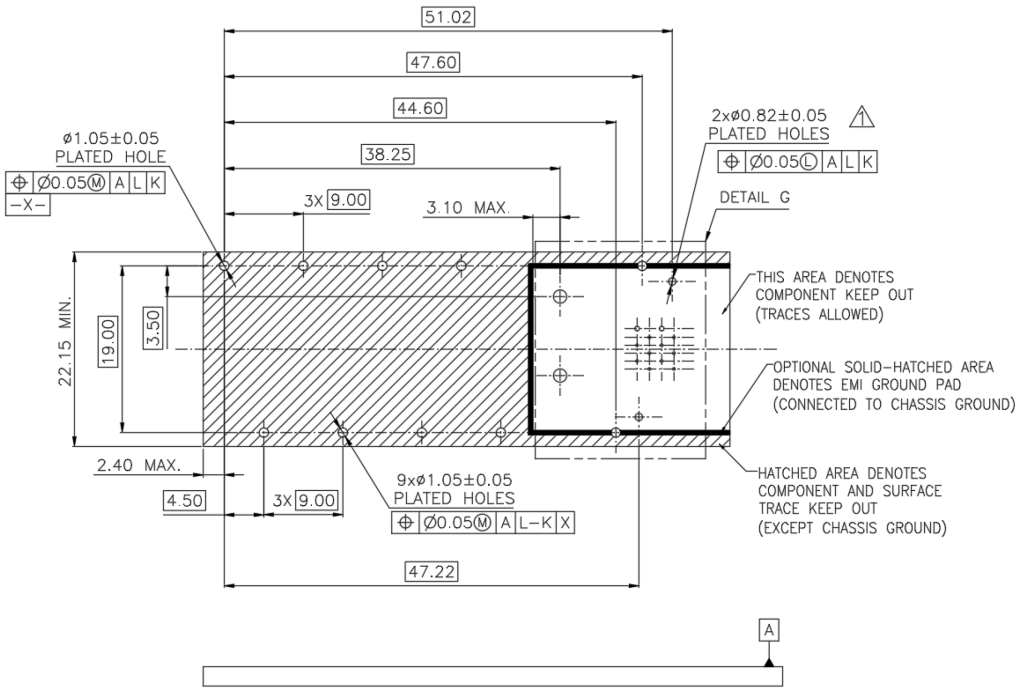


Figure 17 QSFP112 2X1 SMT Connector and cage PCB layout



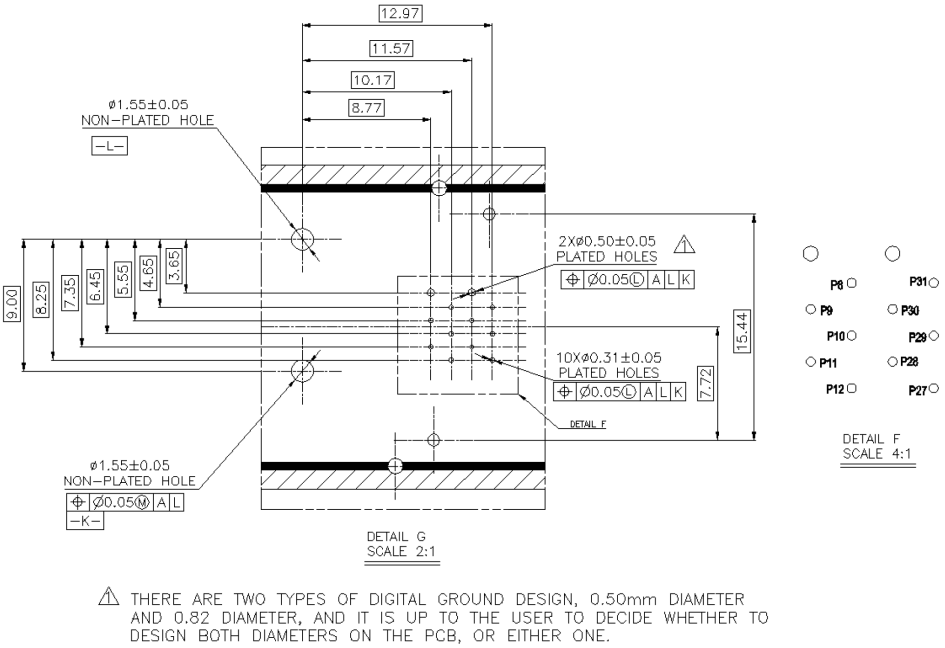
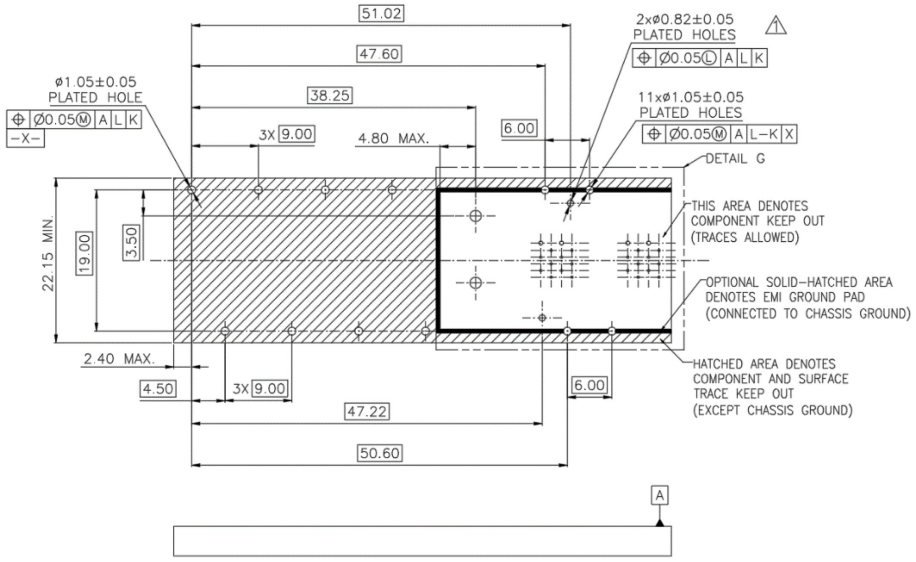


Figure 18 QSFP112 Qpath112 1X1 Connector and cage PCB layout



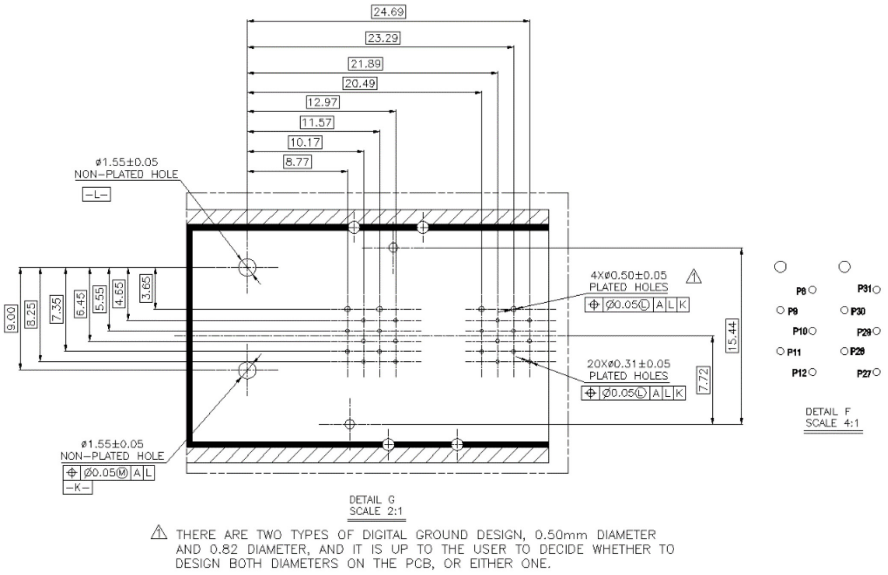


Figure 19 QSFP112 Qpath112 2X1 Connector and cage PCB layout

5.4.1 Insertion, Extraction and Retention Forces for QSFP112 Module

QSFP112 module and cage system insertion, extraction, and retentions forces are given in Table 10. QSFP 112 connector and cage retention system are designed to withstand excessive force applied through the module or cable. The general requirement as applied to the values in the table is that no functional damage shall occur to the module, connector or cage.

Table 10 Insertion, extraction and retention forces for an QSFP112 module

Measurement	Min	Max	Units	Comments
QSFP112 module extraction	0	30	N	EIA-364-13 Test with connector, cage and module. (Latch disengaged, without heatsink)
QSFP112 module insertion	0	60	N	EIA-364-13 Test with connector, cage and module. (Latch disengaged, without heatsink)
QSFP112 module retention	90	NA	N	No functional damage to module
Cage retention (Latch strength)	125	NA	N	No functional damage to latch below 125N
Cage retention in Host Board	114	NA	N	Force to be applied in a vertical direction, no damage to cage
Insertion and removal cycles of connector and cage	100	NA	Cycles	The durability of QSFP112 connector and cage with multiple new modules
Insertion and removal cycles of QSFP112 Module	50	NA	Cycles	The durability of QSFP112 module

5.5 Module Color Coding and Labeling

An exposed feature of the QSFP 112 module (a feature or surface extending outside of the bezel) shall be color coded as follows:

Beige for 850nm
Blue for 1310nm
White for 1550nm

Each QSFP112 module shall be clearly labeled. The complete labeling need not be visible when the QSFP 112 module is installed. The bottom of the device is the recommended location for the label. Labeling shall include:

Appropriate manufacturer and part number identification
Appropriate regulatory compliance labeling
A manufacturing traceability code

The label should also include clear specification of the external port characteristics such as:

Optical wavelength
Required fiber characteristics (i.e. MMF/SMF)
Operating data rate
Interface standards supported
Link length supported
Connector Type

The labeling shall not interfere with the mechanical, thermal or EMI features.

5.6 Bezel for Systems Using QSFP112 Modules

Host enclosures that use QSFP112 devices should provide appropriate clearances between the QSFP112 modules to allow insertion and extraction without the use of special tools and a bezel enclosure with sufficient mechanical strength. See Figure 12 for the recommended bezel designs. The recommended host board thickness for belly-to-belly mounting of the assemblies is 2.2mm minimum.

Applications with host boards less than 2.2 mm minimum will require module dimensions of less than 1.6 mm shown with Note 1 of Figure 12.

The front surface of the cage assembly passes through the bezel. If EMI spring fingers are used, they make contact to the inside of the bezel cutouts. If an EMI gasket is used, it makes contact to the inside surface of the bezel. To accept all cage designs, both bezel surfaces must be conductive and connected to chassis ground.

The recommended basic dimension from the bezel centerline to Datum K and Datum L (See Figure 6 and Figure 12) on the Host board is 43.8mm nominal. The total tolerance can be calculated as follows:

+/- tolerance = 1/2 (bezel thickness) + 0.3mm

For example, a bezel thickness of 1.6mm will have a bezel centerline tolerance of +/- 1.1mm.

The dimension of 43.8 +/- 1.1mm would apply from the Centerline of the bezel to Datums K and L.

The QSFP112 module insertion slot should be clear of nearby moldings and covers that might block convenient access to the latching mechanisms, the QSFP112 module, or the cables connected to the QSFP112 module.

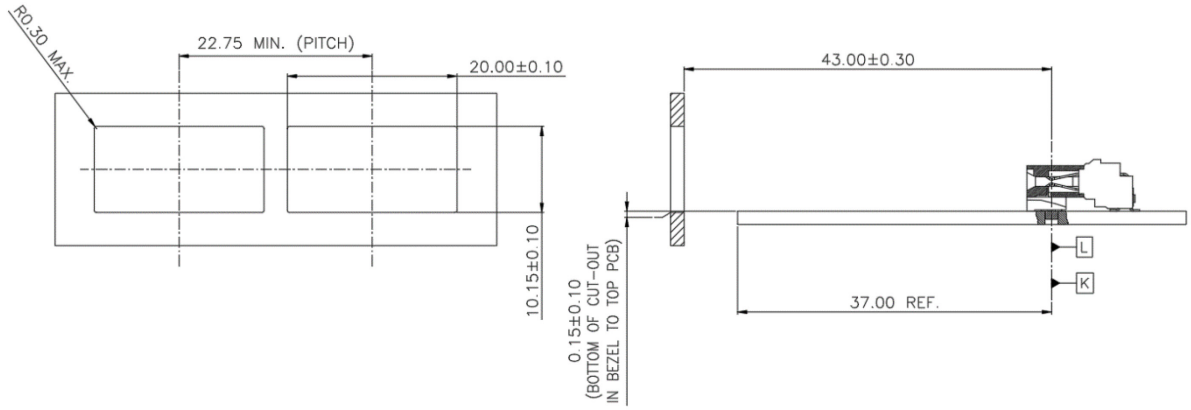


Figure 20 QSFP112 1X1 SMT and Qpath112 Bezel opening

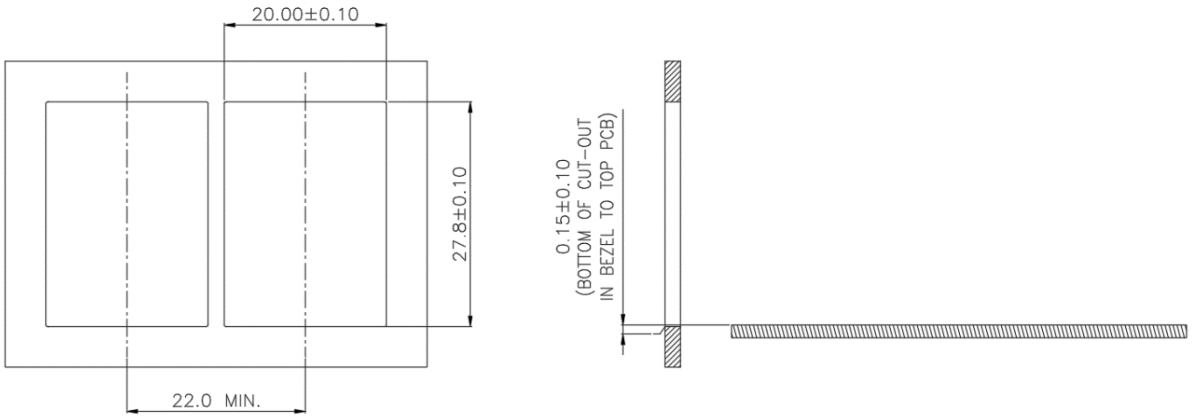


Figure 21 QSFP112 2X1 SMT and Qpath112 Bezel opening

5.7 QSFP112 Electrical Connector Mechanical

The QSFP112 Connector is a 38-contact, right angle surface mount connector and is shown in Figure 22. The mechanical specification for the connector is shown in Figure 23 and Figure 24.

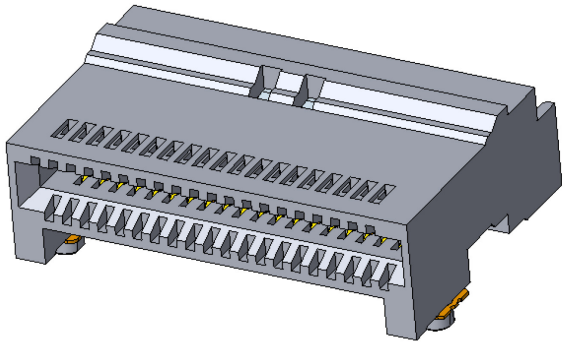


Figure 22 QSFP112 Module electrical connector illustration

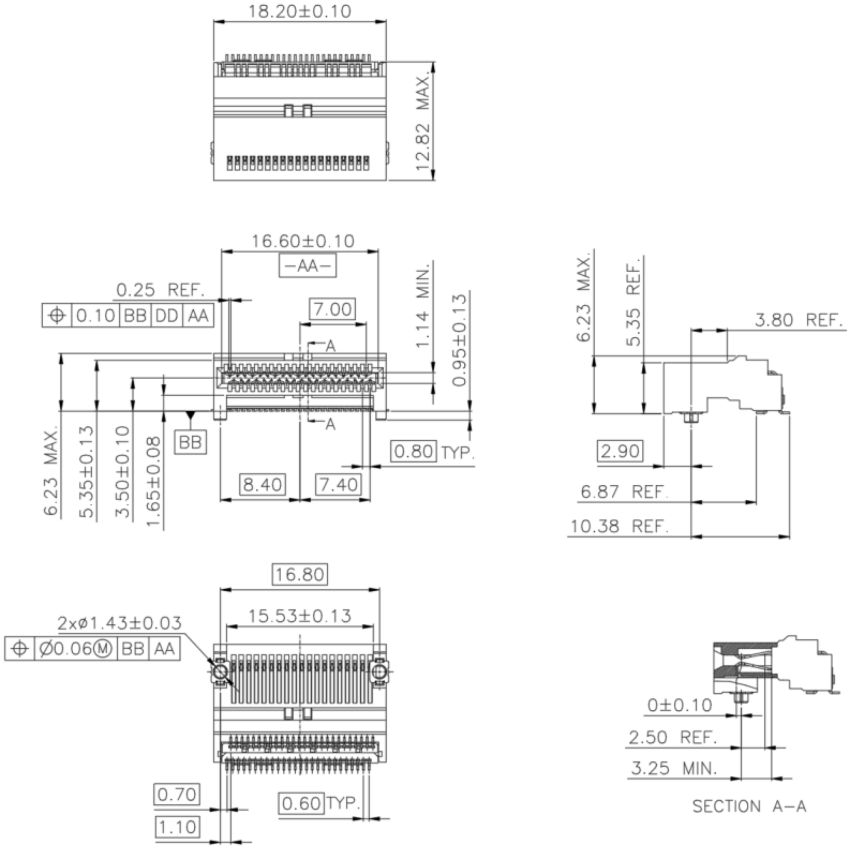


Figure 23 QSFP112 1X1 SMT Connector

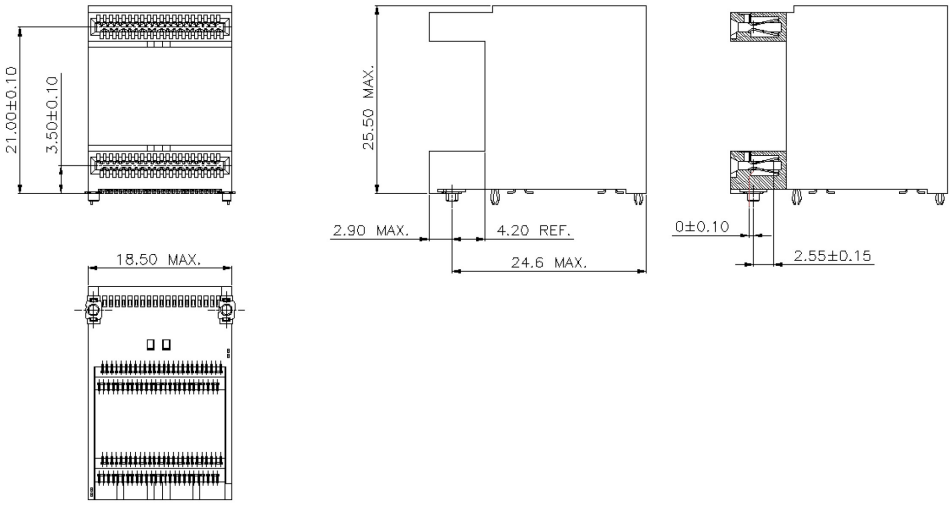


Figure 24 QSFP112 2X1 SMT Connector

5.8 QSFP112 Cage Assembly

The detailed drawings for the cage assembly and reference type of heatsinks are shown in Figure 26, Figure 28, Figure 29 and Figure 30. The 3D reference view of QSFP112 1x1 and 2x1 cage with heat sink and light pipe are shown in Figure 25 and 27. In Figures 25, 27, 29 and 30, the type of heat sinks illustrated are for reference only with the exception of the heat sink base which touches the QSFP module.

For heat sink applications of single cage, the heat sink must be placed on at least one wall of the cage, where it is in contact with or pressed against the module.

For heat sink applications of QSFP112 stacked cage, a heat sink must be placed in the middle channel of the cage, where the heat sink needs to be in contact with or pressed against the module, and the front, side or rear wall of the cage must be provided with a plurality of heat dissipation holes to provide access to the cooling airflow.

For light pipe applications of QSFP112 single cage light pipe, the light pipe is placed adjacent to at least one wall of the cage and must pass through the exterior, interior or intermediate channels of the cage, where the light pipe guides the indicator light source to an indicator light display.

For light pipe applications of QSFP112 stacked cage light pipe, the light pipe is placed adjacent to at least one wall of the cage and must pass through the exterior, interior or intermediate channels of the cage, where the light pipe guides the indicator light source to an indicator light display.

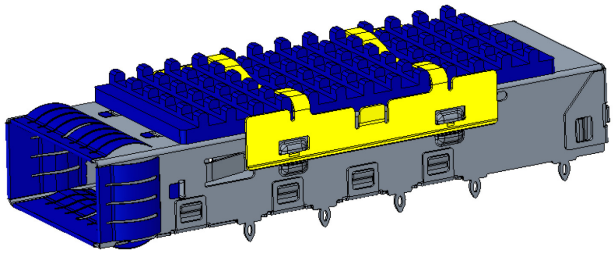


Figure 25 QSFP112 1x1 Cage illustration
(The type of heat sink illustrated is for reference only)

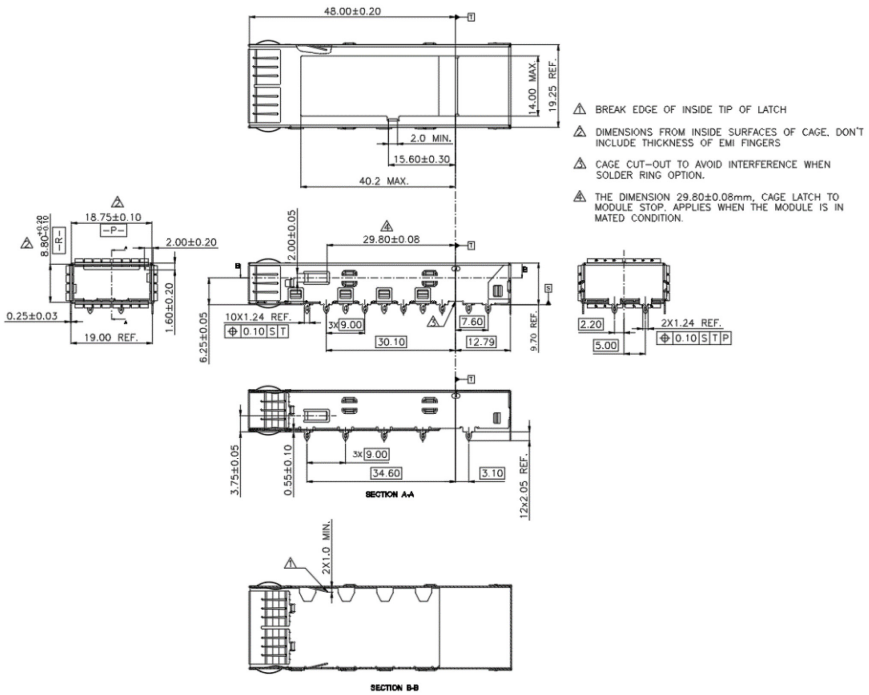


Figure 26 QSFP112 1x1 Cage

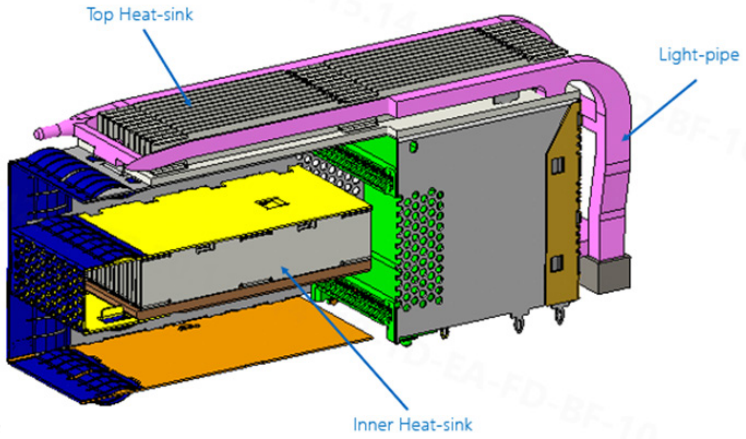


Figure 27 QSFP112 2X1 Cage illustration

(The types of heat sinks illustrated are for reference only)

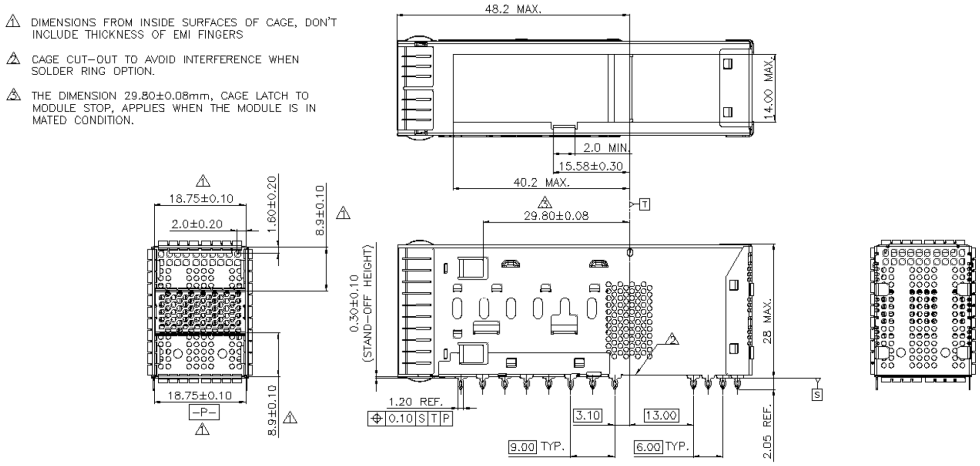


Figure 28 QSFP112 2X1 Cage

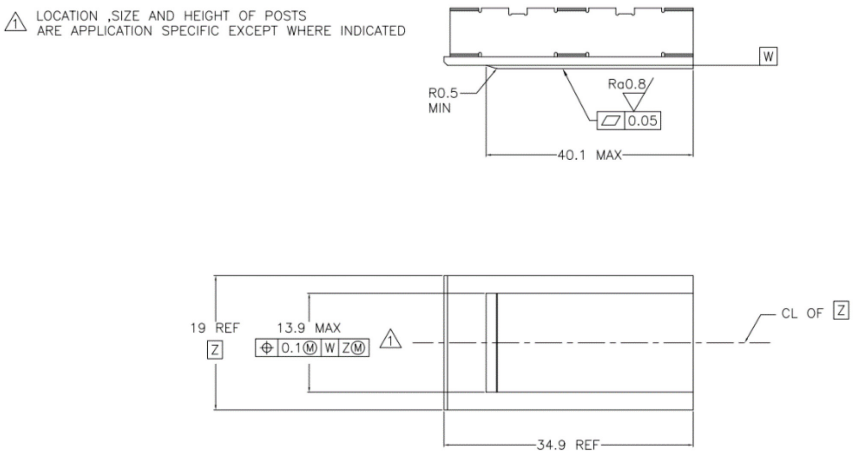


Figure 29 QSFP112 2X1 recommended inner heatsink interface

(The type of heat sink illustrated is for reference only)

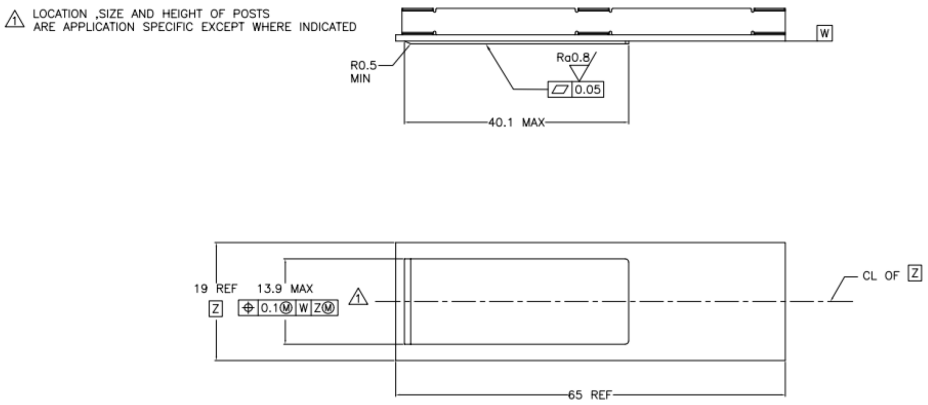


Figure 30 QSFP112 2X1 recommended top heatsink interface

(The type of heat sink illustrated is for reference only)

5.9 QSFP112 Qpath112 Connector and cage

The QSFP112 Qpath112 connector and cage is a 38-contact connector and cage containing high-speed signal contacts that are ultimately connected to cables and low speed and power contacts that are pressed fit to the PCB. The detailed drawings for the Qpath112 connector and cage are shown in Figure 31, Figure 32, Figure 33 and Figure 34.

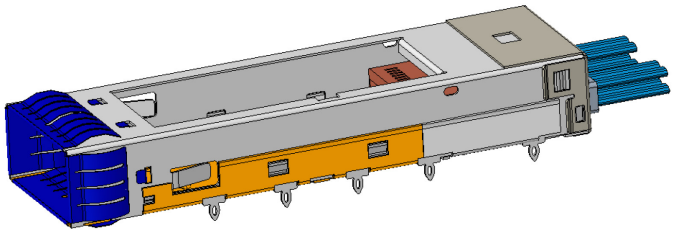


Figure 31 QSFP112 Qpath112 1X1 Connector and cage illustration

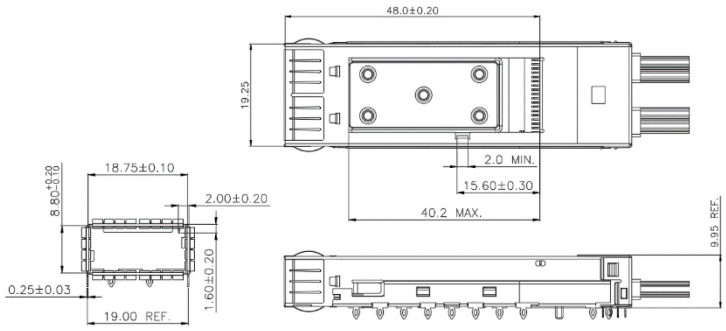


Figure 32 QSFP112 Qpath112 1X1 Connector and cage

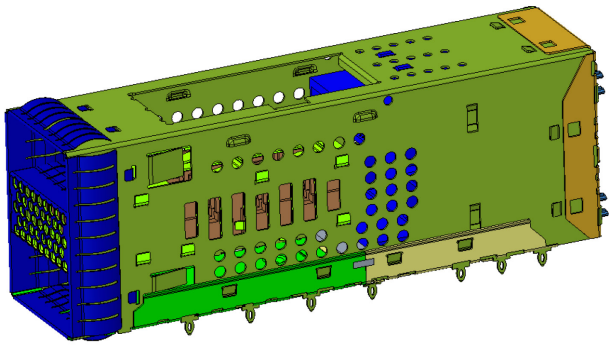


Figure 33 QSFP112 Qpath112 2X1 Connector and cage illustration

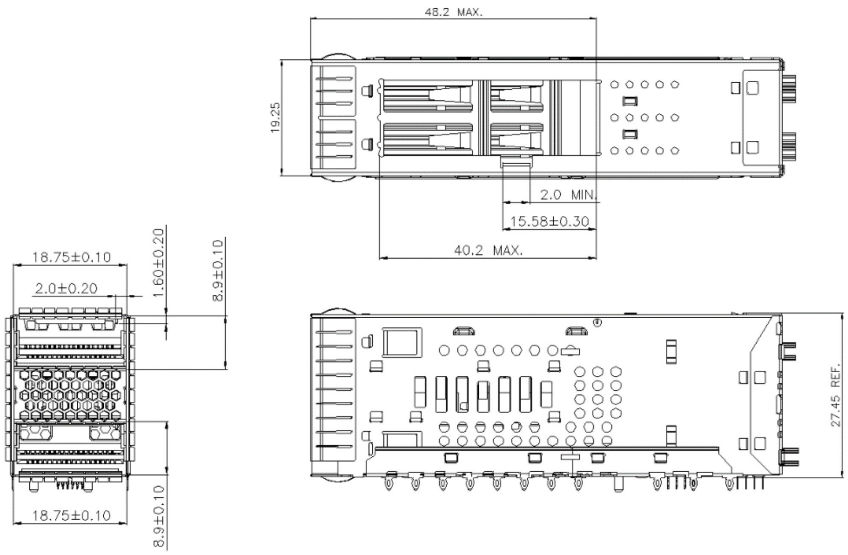


Figure 34 QSFP112 Qpath112 2X1 Connector and cage

5.10 Optical Port Mapping and Optical Interfaces

5.10.1 Electrical data input/output to optical port mapping

The QSFP112 with 4 transmit lanes [Tx1-Tx4] and 4 receive lanes [Rx1-Rx4] allows optical port mapping as shown in Table 11.

Table 11 Electrical Signal to Optical Port Mapping

Electrical data input/output	Optical port mapping (see Figure 35)	
	Duplex LC	MPO-12
	1 TX fiber 1 RX fiber	4 TX fibers 4 RX fibers
Tx1	Tx-1	Tx-1
Tx2		Tx-2
Tx3		Tx-3
Tx4		Tx-4
Rx1	Rx-1	Rx-1
Rx2		Rx-2
Rx3		Rx-3
Rx4		Rx-4

5.10.2 Optical Interfaces

The recommended location and numbering of the optical ports for 3 Media Dependent Interfaces (MDI) are shown in Figure 35. The transmit and receive optical lanes shall occupy the positions depicted in Figure 35 when looking into the MDI receptacle with the connector keyway feature on top. QSFP112 optical MDI examples are shown for a male MPO receptacles (see Figure 36) and a dual LC (see Figure 37).

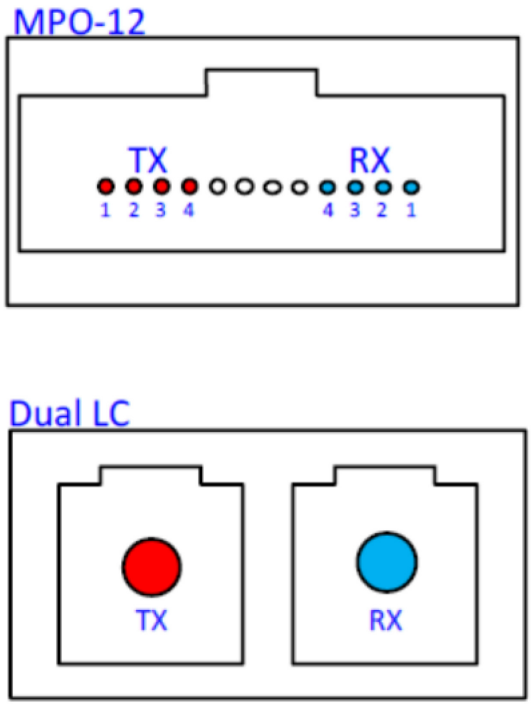


Figure 35 Optical media dependent interface port assignments

5.10.2.1 MPO Optical Cable connections

The optical plug and receptacle for the MPO-12 connectors are specified in TIA-604-5 and shown in Figure 36 (MPO-12 Single Row).
Aligned keys are used to ensure alignment between the modules and the patch cords. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top.
Note: Two alignment pins are present in each receptacle.

Figure 36 MPO-12 One row optical patch cord and module receptacle

5.10.2.2 Dual LC Optical Cable connection

The Dual LC optical patchcord and module receptacle is specified in TIA-604-10 and shown in Figure 37.

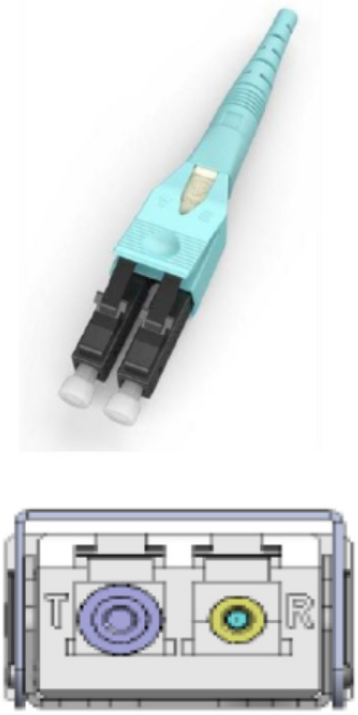


Figure 37 Dual LC optical patchcord and module receptacle

6 Environmental and Thermal

6.1 Temperature Classes

The QSFP112 module shall operate within one or more of the case temperatures ranges defined in Table 12 (a) / Table 12(b). The temperature ranges are applicable between 60m below sea level and 1800m above sea level, (Ref. NEBS GR-63) utilizing the host systems designed airflow.

Table 12 (a) Temperature classification of module case

Class	Case Temperature Range
Standard	0 through 70°C
Extended	-5 through 85°C
Industrial	-40 through 85°C

Table 12 (b) Temperature range classes for tighter controlled applications

Class	Functional Case Temperature	Case Temperature
A1	15 - 60°C	25 - 60°C
A2	5 - 60°C	15 - 60°C
A3	5 - 70°C	15 - 70°C
A4	5 - 75°C	15 - 75°C

6.2 Informative Thermal Design

QSFP112 is designed to allow for up to 16 adjacent modules, ganged and/or belly-to-belly, with the appropriate thermal design for cooling / airflow. (Ref. NEBS GR-63)

For module dimensions all remain the same as the QSFP+/QSFP28 specifications except for the nose protrusion outside of the faceplate of the equipment, Figure 38 shows the four variants of the QSFP112 modules. Type 1 being consistent with the QSFP28 mechanicals and Type 2 having a longer extension beyond the faceplate that module manufacturers can take advantage of for extra design room internal to the module. Type 2A is a further variant on Type 2 which has an integrated heatsink on the nose of the module to facilitate cooling with an efficient secondary heat transfer path. Type 2B increases the height of the nose heatsink to handle higher module power consumption up to 25W. All module variants are compatible with the common QSFP112 connector and cage designs and can be intermixed in a deployment. The main differences listed below.

- Type 1 (same as QSFP28) 72.4 mm max module length
- Type 2 (type1 + 15mm) 87.4mm max module length
- Type 2A (type2 + normal heat sink)
- Type 2B (type2 + enhanced heat sink)

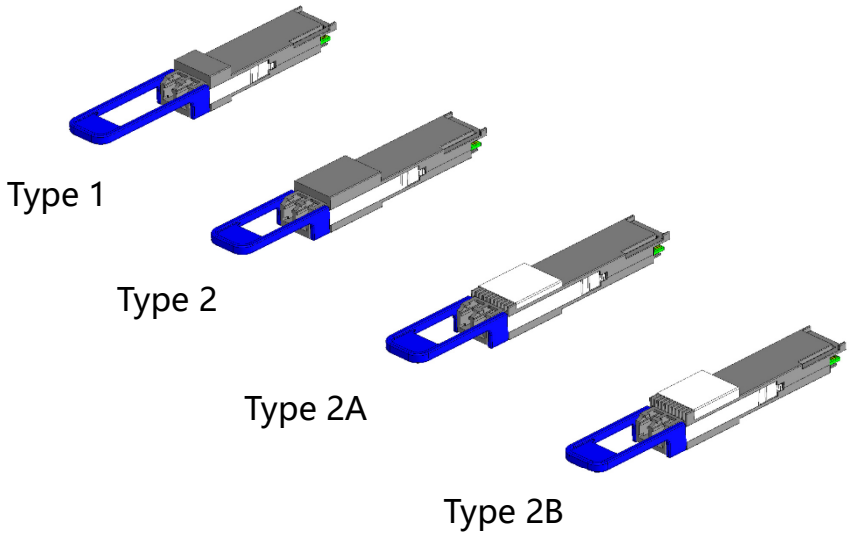


Figure 38 QSFP112 Module variants: Type 1; Type 2; Type 2A; and Type 2B

7 Management Interface

7.1 Introduction

A management interface, as already commonly used in other form factors like QSFP, SFP, is specified in order to enable flexible use of the module by the user. The specification has been changed in order to adopt the use of a multi-channel module. Some timing requirements are critical especially for a multi-channel device, so the interface speed has been increased.

Byte 00h or Byte 128h on Page 00h is used to indicate the use of SFF-8636 or CMIS with 4 host lanes instead of 8 lanes. When a classic QSFP+/QSFP28 module is inserted into a QSFP112 port the host must determine which memory map to use (e.g., SFF-8636 or CMIS) based on the QSFP+ identifier at Byte 00h or Byte 128 Page 00h. The Identifier Value assigned to the module is essential to interpreting the contents of the memory map.

Table 13 Identifier Values

Value	Description of Module
0Dh	QSFP+ or later with SFF-8636 or SFF-8436 management interface (SFF-8436, SFF-8635, SFF-8665, SFF-8685 et al.)
1Eh	QSFP+ or later with Common Management Interface Specification (CMIS)

In some applications, muxing or demuxing may occur in the module. In this specification, all references to lane numbers are based on the electrical connector interface lanes, unless otherwise indicated. In cases where a status or control aspect is applicable only to lanes after muxing or demuxing has occurred, the status or control is intended to apply to all lanes in the mux group, unless otherwise indicated.

7.2 Timing Specification

7.2.1 Introduction

Low speed signaling is based on Low Voltage CMOS (LVCMOS) operating at Vcc. Hosts shall use a pull-up resistor connected to a Vcc_host on the TWI SCL (clock) and SDA (Data) signals. Detailed electrical specification is given in Clause 4.1.2. Nomenclature for all registers more than 1 bit long is MSB-LSB.

7.2.2 Management Interface Timing Specification

The timing parameters for the TWI to the QSFP112 module memory transaction timings are shown in Figure 39 and specified in Table 14 and is compatible with I2C. The default clock rate is a maximum of 400 kHz with an option to support up to a maximum of 1 MHz. This clause closely follows the QSFP+ SFF-8636 specification but with the addition of Fast Mode+. This specification also defines tBUF timing, tWR timing, tNACK timing, tBPC timing.

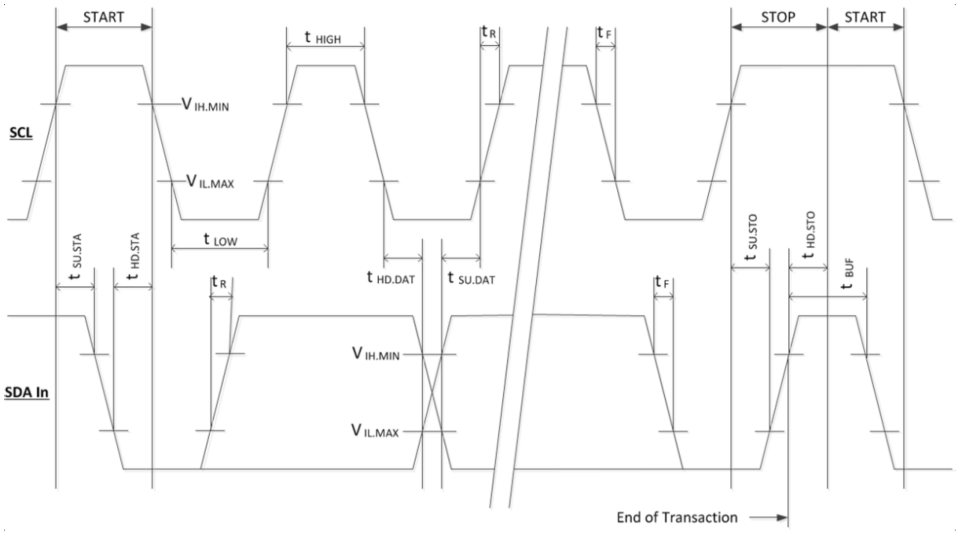


Figure 39 TWI Timing diagram

The TWI serial interface address of the QSFP112 module is 1010000X (A0h). In order to allow access to multiple QSFP modules on the same TWI serial bus, the QSFP112 pinout includes a ModSelL or module select pin. This pin (which is pulled high, deselected in the module) must be held low by the host to select the module of interest and allow communication over the TWI serial interface. The module must not respond to or accept TWI serial bus instructions unless it is selected.
Before initiating a TWI serial bus communication, the host shall provide setup time on the ModSelL line of all modules on the TWI bus. The host shall not change the ModSelL line of any module until the TWI serial bus communication is complete and the hold time requirement is satisfied.

7.2.3 Serial Interface Protocol

The module asserts LOW for clock stretch on SCL.

7.2.3.1 Management Timing Parameters

The timing parameters for the TWI to the QSFP112 module are shown in Table 14.

Table 14 Management interface timing parameters

TWI Modes		Fast Mode (400 kHz)		Fast Mode+ (1MHz)			
Module	Symbol	Min	Max	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	400	0	1000	kHz	
Clock Pulse Width Low	tLOW	1.3		0.50		µs	
Clock Pulse Width High	tHIGH	0.6		0.26		µs	
Time bus free before new transmission can start	tBUF	20		20		µs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		0.26		µs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.6		0.26		µs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		0		µs	
Data In Setup Time	tSU.DAT	0.1		0.1		µs	
Input Rise Time	tR		300		120	ns	From (VL,MAX=0.3*Vcc) to (VIH,MIN=0.7*Vcc)
Input Fall Time	tF		300		120	ns	From (VIH,MIN=0.7*Vcc) to (VIL,MAX=0.3*Vcc)
STOP Setup Time	tSU.STO	0.6		0.26		µs	
STOP Hold Time	tHD.STO	0.6		0.26		µs	
Aborted sequence – bus release	Deselect _Abort		2		2	ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the QSFP112 module releasing SCL and SDA
ModSelL Setup Time[1]	tSU. ModSelL	2		2		ms	ModSelL Setup Time is the setup time on the select line before the start of a host initiated TWI serial bus sequence.
ModSelL Hold Time[1]	tHD. ModSelL	2		2		ms	ModSelL Hold Time is the delay from completion of a TWI serial bus sequence to changes of module select status.
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_ hold		500		500	µs	Time the QSFP112 module may hold the SCL line low before continuing with a read or write operation.
Complete Single or Sequential Write to non- volatile registers	tWR		80		80	ms	Time to complete a Single or Sequential Write to non-volatile registers.
Accept a single or sequential write to volatile memory	tNACK		10		10	ms	Time to complete a Single or Sequential Write to volatile registers.
Time to complete a memory bank/page	tBPC		10		10	ms	Time to complete a memory bank and/or page change.
Endurance (Write Cycles)		50k		50k		cycles	Module Case Temperature = 70 ºC

Note 1: The management registers can be read to determine alternate support for ModSelL set up and hold times. See CMIS 8.4.5, Durations Advertising or SFF-8636 6.2.9, Free Side Device Properties (Page 00h, Bytes 107-115).

7.3 Timing for Soft Control and Status Functions

Timing for QSFP112 soft control and status functions are described in Table 15.

Table 15 I/O Timing for soft control and status functions

Parameter	Symbol	Min	Max	Unit	Conditions
MgmtInit Duration	Max MgmtInit Duration		2000	ms	Time from power on [1], hot plug or rising edge of reset until the high to low SDA transition of the Start condition for the first acknowledged TWI transaction.
ResetL Assert Time	t_reset_init	10		µs	Minimum pulse time on the ResetL signal to initiate a module reset.
Int/RxLOS Mode Change	t_IntL/RxLOSL		100	ms	Time to change between IntL and RxLOSL modes of the dual- mode signal IntL/RxLOSL.
LPMode/TxDis mode change time	t_LPMode/TxDis		100	ms	Time to change between LPMode and TxDis modes of LPMode/TxDis
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read [2] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
RxLOS Assert Time	ton_los		100	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted [3].
Rx LOS Assert Time (optional fast mode)	ton_losf		1	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted [3].
RxLOS Deassert Time (optional fast mode)	toff_f_LOS		3	ms	Optional fast mode is advertised via the CMIS. Time from optical signal above the LOS deassert threshold to when the module releases the RxLOSL signal to high.
TX Disable Assert Time	ton_TxDis		100	ms	Time from Tx Disable bit set to 1 until optical output falls below 10% of nominal.
TX Disable Assert Time (optional fast mode)	ton_f_TxDis		3	ms	Optional fast mode is advertised via CMIS. Time from TxDis signal high to the optical output reaching the disabled level
TX Disable Deassert Time	toff_TxDis		400	ms	Time from Tx Disable bit cleared to 1 until optical output rises above 90% of nominal [4].
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b) [5] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b) [5] until associated IntL operation resumes
Data Path Tx Turn On Max Duration [6]	DataPathTxTurnOn_MaxDuration				see CMIS memory P01h: B168
Data Path Tx Turn Off Max Duration [6]	DataPathTxTurnOff_MaxDuration				see CMIS memory P01h: B168
Data Path Deinit Max Duration [6]	DataPathDeinit_MaxDuration				see CMIS memory P01h: B144
Data Path Init Max Duration [6]	DataPathInit_MaxDuration				see CMIS memory P01h: B144

Module Pwr Up Max Duration [7]	ModulePwrUp_MaxDuration	see CMIS memory P01h: B167
Module Pwr Dn Max Duration [7]	ModulePwrDn_MaxDuration	see CMIS memory P01h: B167

Notes:
1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 7.
2. Measured from low to high SDA edge of the Stop condition of the read transaction.
3. Rx LOS condition is defined at the optical input by the relevant standard.
4. Tx Squelch Deassert time is longer than SFF-8679.
5. Measured from low to high SDA edge of the Stop condition of the write transaction.
6. Measured from the low to high SDA edge of the Stop condition of the Write transaction until the IntL for the state change Vout:IntL=Vol, unless the module advertises a less than 1 ms duration in which case there is no defined measurement.
7. Measured from the low to high SDA edge of the Stop condition of the Write transaction until the IntL for the state change Vout:IntL=Vol.

Squelch and disable timings are defined in Table 16.

Table 16 I/O Timing for squelch and disable

Parameter	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	15	ms	Time from loss of Rx input signal until the squelched output condition is reached. See clause 4.1.3.1.
Rx Squelch Deassert Time	toff_Rxsq	80	us	Time from resumption of Rx input signals until normal Rx output condition is reached. See clause 4.1.3.1.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached. See clause 4.1.3.2.
Tx Squelch Deassert Time	toff_Txsq	1.5	s	Time from resumption of Tx input signals until normal Tx output condition is reached. See clause 4.1.3.2.
Tx Disable Assert Time	ton_txdis	100	ms	Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal, see notes 2 and 3.
Tx Disable Deassert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal, see notes 2 and 3.
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal
Rx Output Disable Deassert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set (value = 1b)[1] until squelch functionality is disabled.
Squelch Disable Deassert Time	toff_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled.
Note 1. Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction.				
Note 2. CMIS 5.0 and beyond the listed values are superseded by the advertised DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn_MaxDuration times in P01h.168.				
Note 3. Listed values place a limit on the DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn_MaxDuration times (P01h.168) that can be advertised by such modules (for CMIS 5.0 and beyond).				

7.4 Device Addressing and Operation

Serial Clock (SCL): The host supplied SCL input to QSFP112 modules is used to positive-edge clock data into each QSFP112 device and negative-edge clock data out of each device. The SCL line may be pulled low by an QSFP112 module during clock stretching.
Serial Data (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain or open-collector driven and may be wire-ORed with any number of open-drain or open collector devices.
Master/Slave: QSFP112 modules operate only as slave devices. The host must provide a bus master for SCL and initiate all read/write communication.
Device Address: Each QSFP112 is hard wired at the device address A0h. See Clause 7.6 for memory structure within each module.
Multiple Devices per SCL/SDA: While QSFP112 modules are compatible with point-to-point SCL/SDA, they can share a single SCL/SDA bus by using the QSFP112 ModSelL line. See Clause 4.1.1,Clause 4.1.2 , Table 3 for more information.
Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicate a START or STOP condition. All addresses and data words are serially transmitted to and from the QSFP112 in 8-bit words.
Every byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.
START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.
STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.
Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Device address bytes and write data bytes initiated by the host shall be acknowledged by QSFP112 modules.
Read data bytes transmitted by QSFP112 modules shall be acknowledged by the host for all but the final byte read, for which the host shall respond with a STOP instead of an ACK.
Memory (Management Interface) Reset: After an interruption in protocol, power loss or system reset the QSFP112 management interface can be reset. Memory reset is intended only to reset the QSFP112 module management interface (to correct a hung bus). No other module functionality is implied.

1) Clock up to 9 cycles.
2) Look for SDA high in each cycle while SCL is high.
3) Create a START condition as SDA is high

Device Addressing: QSFP112 devices require an 8-bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory sequence for the first seven most significant bits in Figure 40. This is common to all QSFP112 devices.

1	0	1	0	0	0	0	R/W
MSB							LSB

Figure 40 QSFP112 Device address

The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low. Upon compare of the device address (with ModSelL in the low state) the QSFP112 module shall output a zero (ACK) on the SDA line to acknowledge the address.

7.5 Read/Write Functionality

7.5.1 QSFP112 Memory Address Counter (Read AND Write Operations)

QSFP112 devices maintain an internal data word address counter containing the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the module. This address stays valid between operations as long as QSFP112 power is maintained. The address "roll over" during read and writes operations is from the last byte of the 128-byte memory page to the first byte of the same page.

7.5.2 Read Operations (Current Address Read)

A current address read operation requires only the device address read word (10100001) be sent, see Figure 41. Once acknowledged by the QSFP112, the current address data word is serially clocked out. The host does not respond with an acknowledge, but does generate a STOP condition once the data word is read.

		<-- QSFP112 ADDR -->																		
HOST	START	MSB						LSB	READ										NACK	STOP
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
QSFP										ACK	MSB							LSB		
											<---DATA WORD--->									

Figure 41 QSFP112 Current address read operation

7.5.3 Read Operations (Random Read)

A random read operation requires a "dummy" write operation to load in the target byte address as shown in Figure 42. This is accomplished by the following sequence: The target 8-bit data word address is sent following the device address write word (10100000) and acknowledged by the QSFP112. The host then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read address (10100001). The QSFP112 acknowledges the device address and serially clocks out the requested data word. The host does not respond with an acknowledge, but does generate a STOP condition once the data word is read.

		<-- QSFP112 ADDR -->									<--MEMORY ADDR->										<QSFP112 ADDR->																		
HOST	START	MSB						LSB	WRITE		MSB							LSB		START	MSB						LSB	READ										NACK	STOP
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
QSFP										ACK									ACK										ACK	MSB							LSB		
																														<DATA WORD n-->									

Figure 42 QSFP112 Random read

7.5.3.1 Read Operations (Sequential Read)

Sequential reads are initiated by either a current address read (Figure 43) or a random address read (Figure 44). To specify a sequential read, the host responds with an acknowledge (instead of a STOP) after each data word. As long as the QSFP112 receives an acknowledge, it shall serially clock out sequential data words. The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledge.

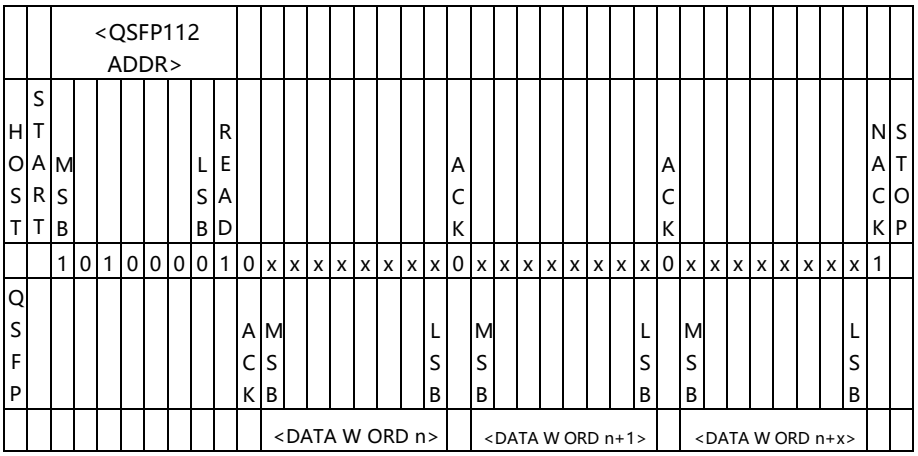


Figure 43 Sequential address read starting at QSFP112 current address•

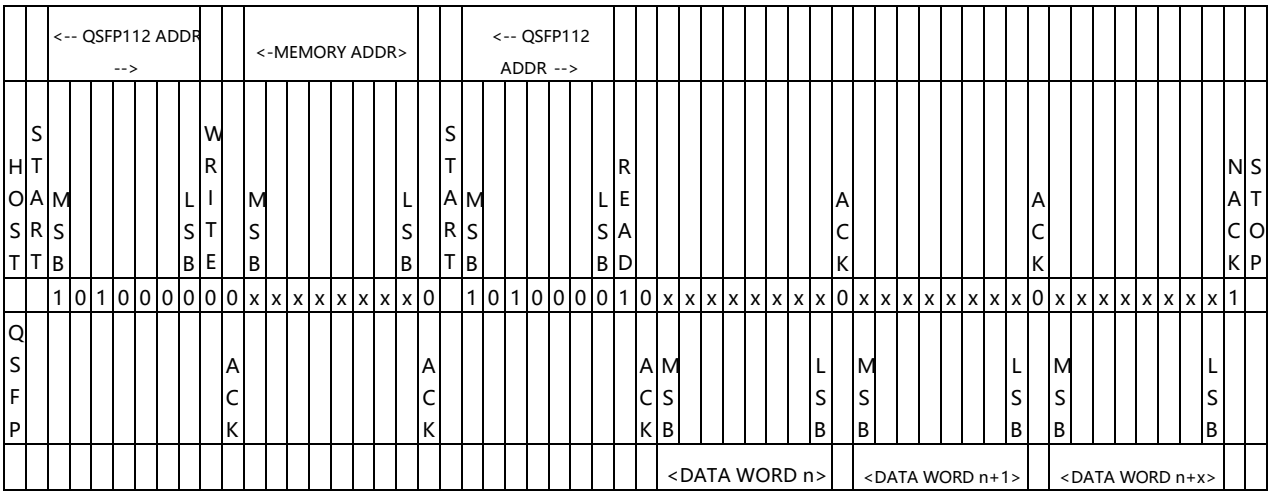


Figure 44 Sequential address read starting with random QSFP112 read

7.5.4 Write Operations (BYTE Write)

A write operation requires an 8-bit data word address following the device address write word (10100000) and acknowledgement, see Figure 45. Upon receipt of this address, the QSFP112 shall again respond with a zero (ACK) to acknowledge and then clock in the first 8-bit data word. Following the receipt of the 8-bit data word, the QSFP112 shall output a zero (ACK) and the host master must terminate the write sequence with a STOP condition for the write cycle to begin. If a START condition is sent in place of a STOP condition (i.e. a repeated START per the TWI specification) the write is aborted and the data received during that operation is discarded. Upon receipt of the proper STOP condition, the QSFP112 enters an internally timed write cycle, t_{WR}, to internal memory. The QSFP112 disables it is management interface input during this write cycle and shall not respond or acknowledge subsequent commands until the write is complete. Note that TWI "Combined Format" using repeated START conditions is not supported on QSFP112 write commands.

		<-- QSFP112 ADDR -->								<-MEMORY ADDR->								<-- DATA WORD -->									
HOST	START	MSB							LSB	WRITE	MSB						LSB		MSB						LSB		STOP
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
QSFP										ACK									ACK								ACK	

Figure 45 QSFP112 Write byte operation

7.5.5 Write Operations (Sequential Write)

QSFP shall support up to a 4 sequential byte write without repeatedly sending QSFP112 address and memory address information as shown in Figure 46. A "sequential" write is initiated the same way as a single byte write, but the host master does not send a stop condition after the first word is clocked in. Instead, after the QSFP112 acknowledges receipt of the first data word, the host can transmit up to three more data words. The QSFP112 shall send an acknowledge after each data word received. The host must terminate the sequential write sequence with a STOP condition or the write operation shall be aborted and data discarded. Note that TWI "combined format" using repeated START conditions is not supported on QSFP112 write commands.

		<- QSFP112 ADDR ->									<MEMORY ADDR>									<--DATA WORD 1->									<--DATA WORD 2->									<--DATA WORD 3->									<-DATA WORD 4-->									
HOST	START	MSB							LSB	WRITE	MSB								LSB		MSB								LSB		MSB								LSB		MSB								LSB		MSB								LSB		STOP
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
QSFP										ACK									ACK									ACK									ACK									ACK									ACK	

Figure 46 QSFP112 Sequential write operation

7.5.6 Write Operations (Acknowledge Polling)

Once the QSFP112 internally timed write cycle has begun (and inputs are being ignored on the bus) acknowledge polling can be used to determine when the write operation is complete. This involves sending a START condition followed by the device address word. Only if the internal write cycle is complete shall the QSFP112 respond with an acknowledge to subsequent commands, indicating read or write operations can continue.

7.6 QSFP112 Memory Map

QSFP112 management interface, as already commonly used in other form factors like QSFP and SFP, is specified in order to enable flexible use of the module by the user. The memory map for QSFP112 is found in "Common Management Interface Specification (CMIS 5.0) or later".

Appendix A

Several informative designs examples of higher power Type 2A and 2B QSFP112 with integrated nose heat sinks are shown in Figure 47, Figure 48, and Figure 49.

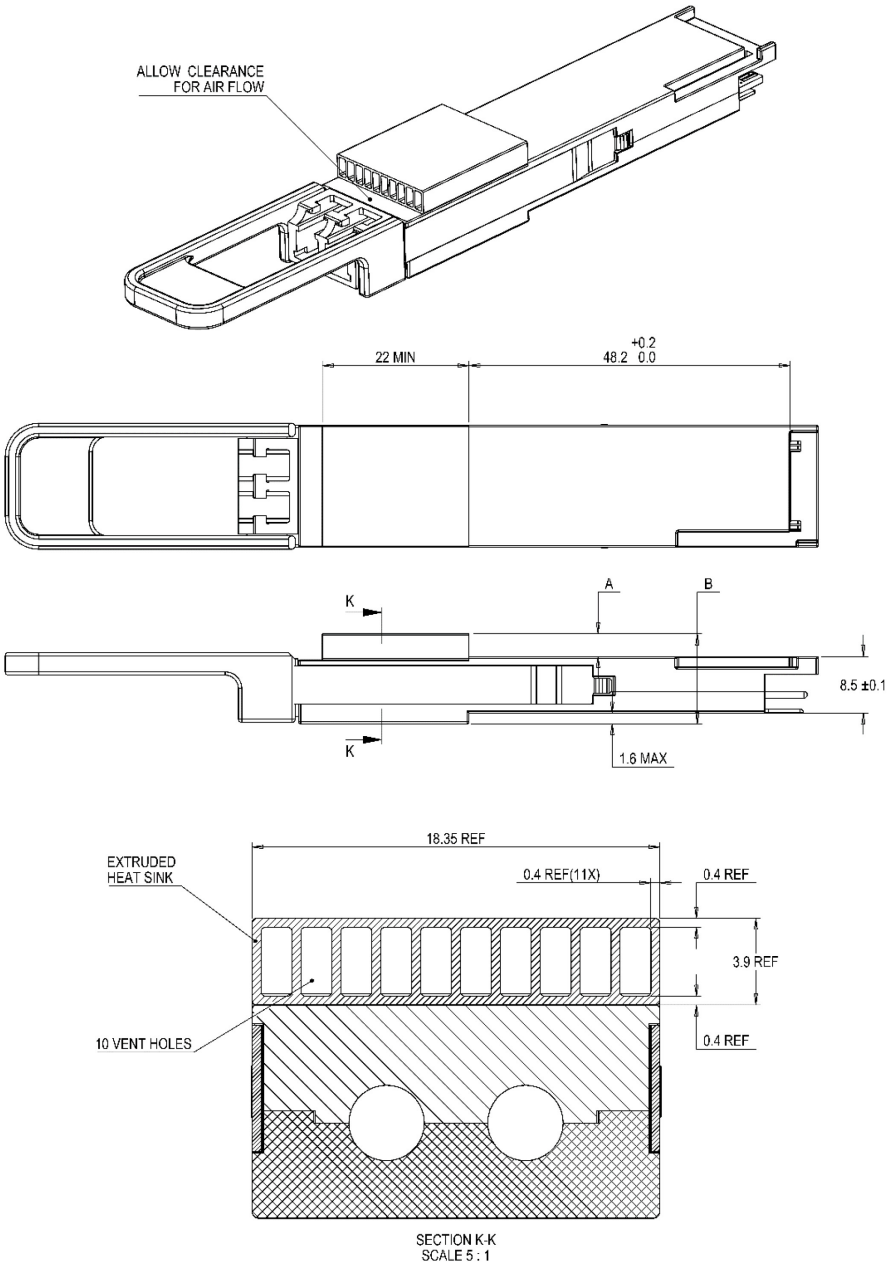


Figure 47 Type 2A and 2B examples of extruded Heat Sink Example

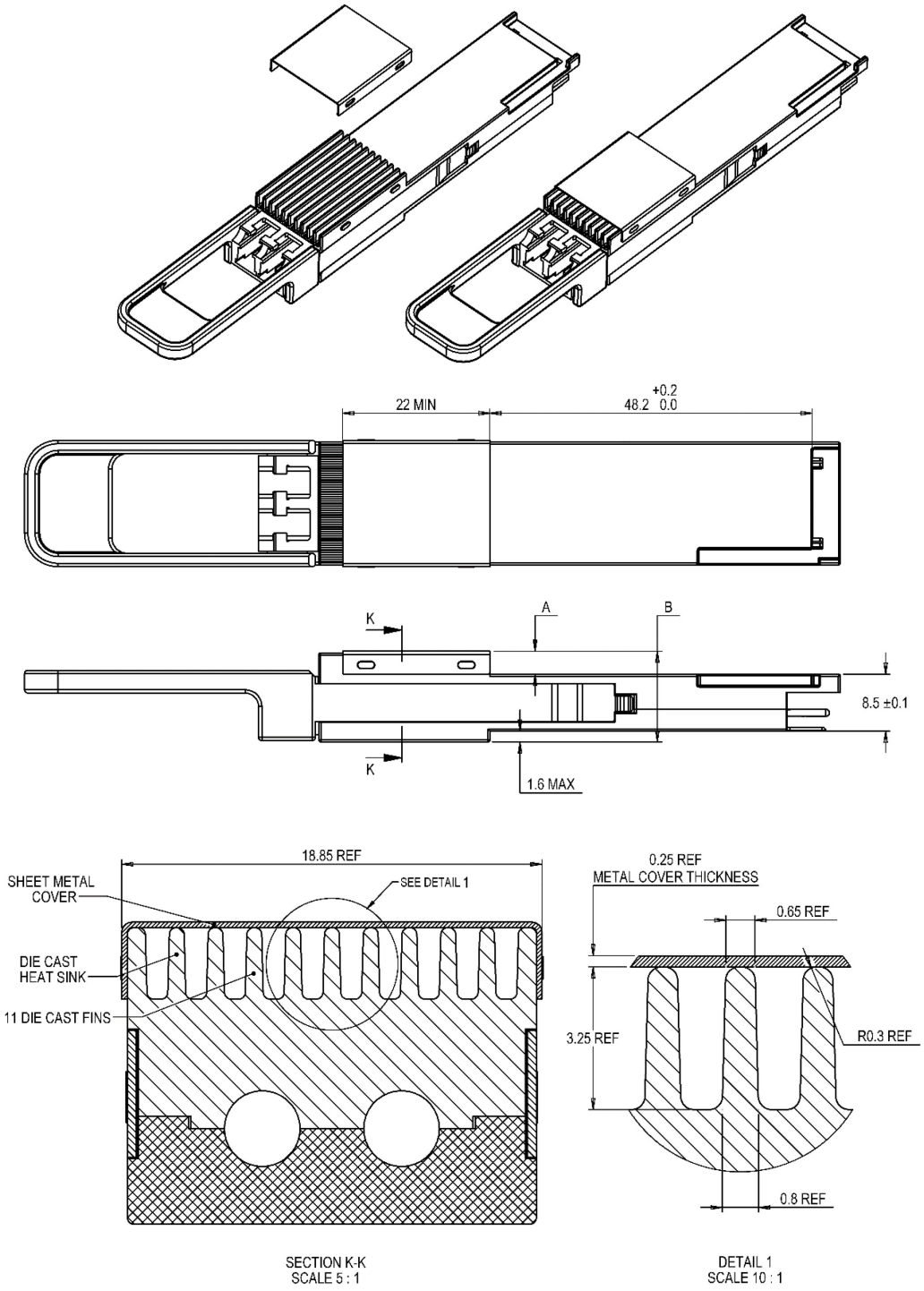


Figure 48 Type 2A and 2B examples of die Cast Heat Sink Example

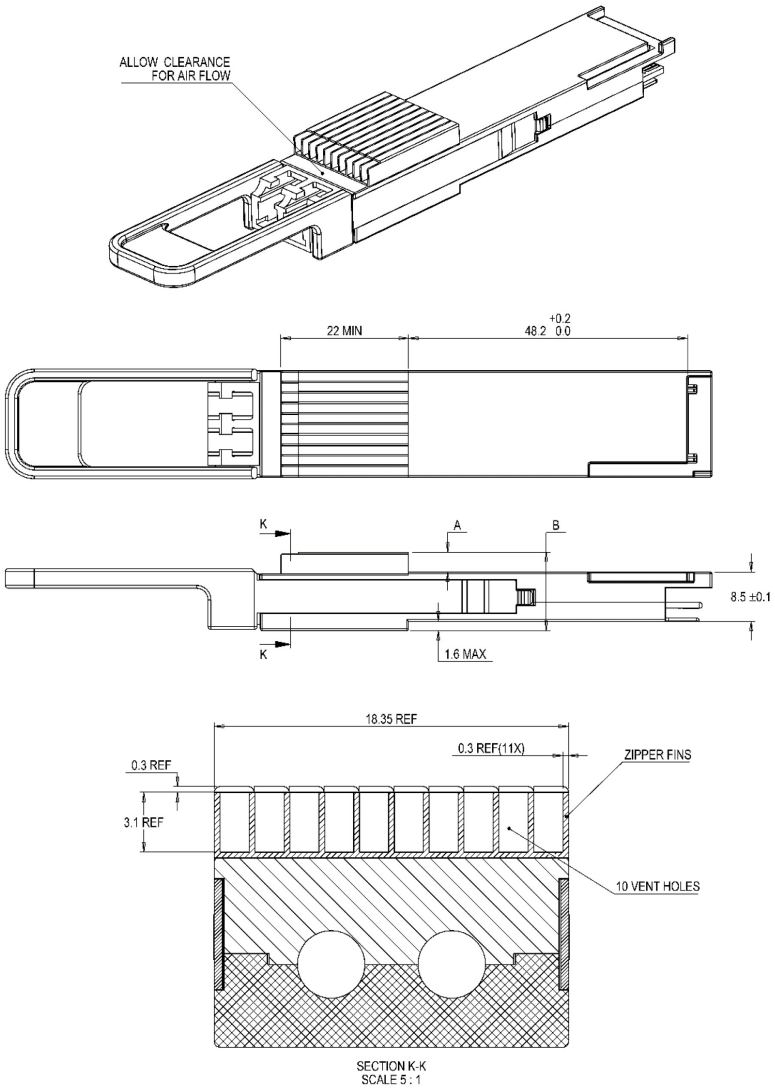


Figure 49 Type 2A and 2B examples of zipper Fin Heat Sink Example

Thermal design is system dependent; however, systems seeking to maximize the benefit of the external heat sink of Type 2A and 2B modules should consider minimizing bypass of airflow through the external heat sink. Type 2A and 2B modules have a heat sink on the nose of the module. The QSFP112 type 2B modules are taller and can only be used in special stack cages as the ports on a thermal enhanced stacked QSFP112 cage are separated by 1.7mm more than normal QSFP112 stack cages. However, a Type 2A module can be used in all applications.

Type 2A and Type 2B extruded heat sink examples are shown in Figure 47. Type 2A and Type 2B die cast heat sinks with metal cover examples are shown in Figure 48. Type 2A and Type 2B zipper fin heat sink examples are shown in Figure 49. Dimensions A, B for Type 2A and 2B heat sinks in Figure 47, Figure 48, and Figure 49 are given in Table 17. All dimensions shall have dimension tolerance of +/-0.1 mm.

Table 17 Informative Dimensions for QSFP112 Module Type 2A/2B

Dimensions	Module Type 2A	Module Type 2B
A (max)	3.4 mm	5.1 mm
B (REF)	13.5 mm	15.2 mm